

Description

Atmel's SAM3S series is a member of a family of 32-bit Flash microcontrollers based on the high performance ARM Cortex-M3 processor. It operates at a maximum speed of 64 MHz and features up to 256 Kbytes of Flash and up to 48 Kbytes of SRAM. The peripheral set includes a Full Speed USB Device port with embedded transceiver, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface featuring a Static Memory Controller providing connection to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, 2x USARTs, 2x UARTs, 2x TWIs, 3x SPI, an I2S, as well as 1 PWM timer, 6x general-purpose 16-bit timers, an RTC, an ADC, a 12-bit DAC and an analog comparator.

The SAM3S series is ready for capacitive touch thanks to the QTouch library, offering an easy way to implement buttons, wheels and sliders

The SAM3S device is a medium range general purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set. This enables the SAM3S to sustain a wide range of applications including consumer, industrial control, and PC peripherals.

It operates from 1.62V to 3.6V and is available in 48-, 64- and 100-pin QFP, 48- and 64-pin QFN, and 100-pin BGA packages.

The SAM3S series is the ideal migration path from the SAM7S series for applications that require more performance. The SAM3S series is pin-to-pin compatible with the SAM7S series.

This is a summary document.
The complete document is
available on the Atmel website
at www.atmel.com.

1. Features

- Core
 - ARM® Cortex®-M3 revision 2.0 running at up to 64 MHz
 - Memory Protection Unit (MPU)
 - Thumb®-2 instruction set
- Pin-to-pin compatible with AT91SAM7S series (48- and 64-pin versions)
- Memories
 - From 64 to 256 Kbytes embedded Flash, 128-bit wide access, memory accelerator, single plane
 - From 16 to 48 Kbytes embedded SRAM
 - 16 Kbytes ROM with embedded bootloader routines (UART, USB) and IAP routines
 - 8-bit Static Memory Controller (SMC): SRAM, PSRAM, NOR and NAND Flash support
 - Memory Protection Unit (MPU)
- System
 - Embedded voltage regulator for single supply operation
 - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation
 - Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with Failure Detection and optional low power 32.768 kHz for RTC or device clock
 - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment
 - Slow Clock Internal RC oscillator as permanent low-power mode device clock
 - Two PLLs up to 130 MHz for device clock and for USB
 - Temperature Sensor
 - Up to 22 peripheral DMA (PDC) channels
- Low Power Modes
 - Sleep and Backup modes, down to 1.8 µA in Backup mode
 - Ultra low power RTC
- Peripherals
 - USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints. On-Chip Transceiver
 - Up to 2 USARTs with ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Mode
 - Two 2-wire UARTs
 - Up to 2 Two Wire Interface (I2C compatible), 1 SPI, 1 Serial Synchronous Controller (I2S), 1 High Speed Multimedia Card Interface (SDIO/SD Card/MMC)
 - Up to 6 Three-Channel 16-bit Timer/Counter with capture, waveform, compare and PWM mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
 - 4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control
 - 32-bit Real-time Timer and RTC with calendar and alarm features
 - Up to 15-channel, 1Msps ADC with differential input mode and programmable gain stage
 - One 2-channel 12-bit 1Msps DAC
 - One Analog Comparator with flexible input selection, Selectable input hysteresis
 - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)
 - Write Protected Registers
- I/O
 - Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
 - Three 32-bit Parallel Input/Output Controllers, Peripheral DMA assisted Parallel Capture Mode
- Packages
 - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/100-ball TFBGA, 9 x 9 mm, pitch 0.8 mm
 - 64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/64-pad QFN 9x9 mm, pitch 0.5 mm
 - 48-lead LQFP, 7 x 7 mm, pitch 0.5 mm/48-pad QFN 7x7 mm, pitch 0.5 mm

1.1 Configuration Summary

The SAM3S microcontrollers differ in memory size, package and features list. [Table 1-1](#) below summarizes the configurations of the device family

Table 1-1. Configuration Summary

| Device | Flash | SRAM | Timer Counter Channels | GPIOs | UART/ USARTs | ADC | 12-bit DAC Output | External Bus Interface | HSMCI | Package |
|---------|-------------------------|-----------|------------------------|-------|--------------------|--------|-------------------|--|---------------|----------------|
| SAM3S4C | 256 Kbytes single plane | 48 Kbytes | 6 | 79 | 2/2 ⁽¹⁾ | 15 ch. | 2 | 8-bit data, 4 chip selects, 24-bit address | 1 port 4 bits | LQFP100 BGA100 |
| SAM3S4B | 256 Kbytes single plane | 48 Kbytes | 3 | 47 | 2/2 ⁽¹⁾ | 10 ch. | 2 | - | 1 port 4 bits | LQFP64 QFN 64 |
| SAM3S4A | 256 Kbytes single plane | 48 Kbytes | 3 | 34 | 2/1 | 8 ch. | - | - | - | LQFP48 QFN 48 |
| SAM3S2C | 128 Kbytes single plane | 32 Kbytes | 6 | 79 | 2/2 ⁽¹⁾ | 15 ch. | 2 | 8-bit data, 4 chip selects, 24-bit address | 1 port 4 bits | LQFP100 BGA100 |
| SAM3S2B | 128 Kbytes single plane | 32 Kbytes | 3 | 47 | 2/2 ⁽¹⁾ | 10 ch. | 2 | - | 1 port 4 bits | LQFP64 QFN 64 |
| SAM3S2A | 128 Kbytes single plane | 32 Kbytes | 3 | 34 | 2/1 | 8 ch. | - | - | - | LQFP48 QFN 48 |
| SAM3S1C | 64 Kbytes single plane | 16 Kbytes | 6 | 79 | 2/2 ⁽¹⁾ | 15 ch. | 2 | 8-bit data, 4 chip selects, 24-bit address | 1 port 4 bits | LQFP100 BGA100 |
| SAM3S1B | 64 Kbytes single plane | 16 Kbytes | 3 | 47 | 2/2 ⁽¹⁾ | 10 ch. | 2 | - | 1 port 4 bits | LQFP64 QFN 64 |
| SAM3S1A | 64 Kbytes single plane | 16 Kbytes | 3 | 34 | 2/1 | 8 ch. | - | - | - | LQFP48 QFN 48 |

Note: 1. Full Modem support on USART1.

2. SAM3S Block Diagram

Figure 2-1. SAM3S 100-pin Version Block Diagram

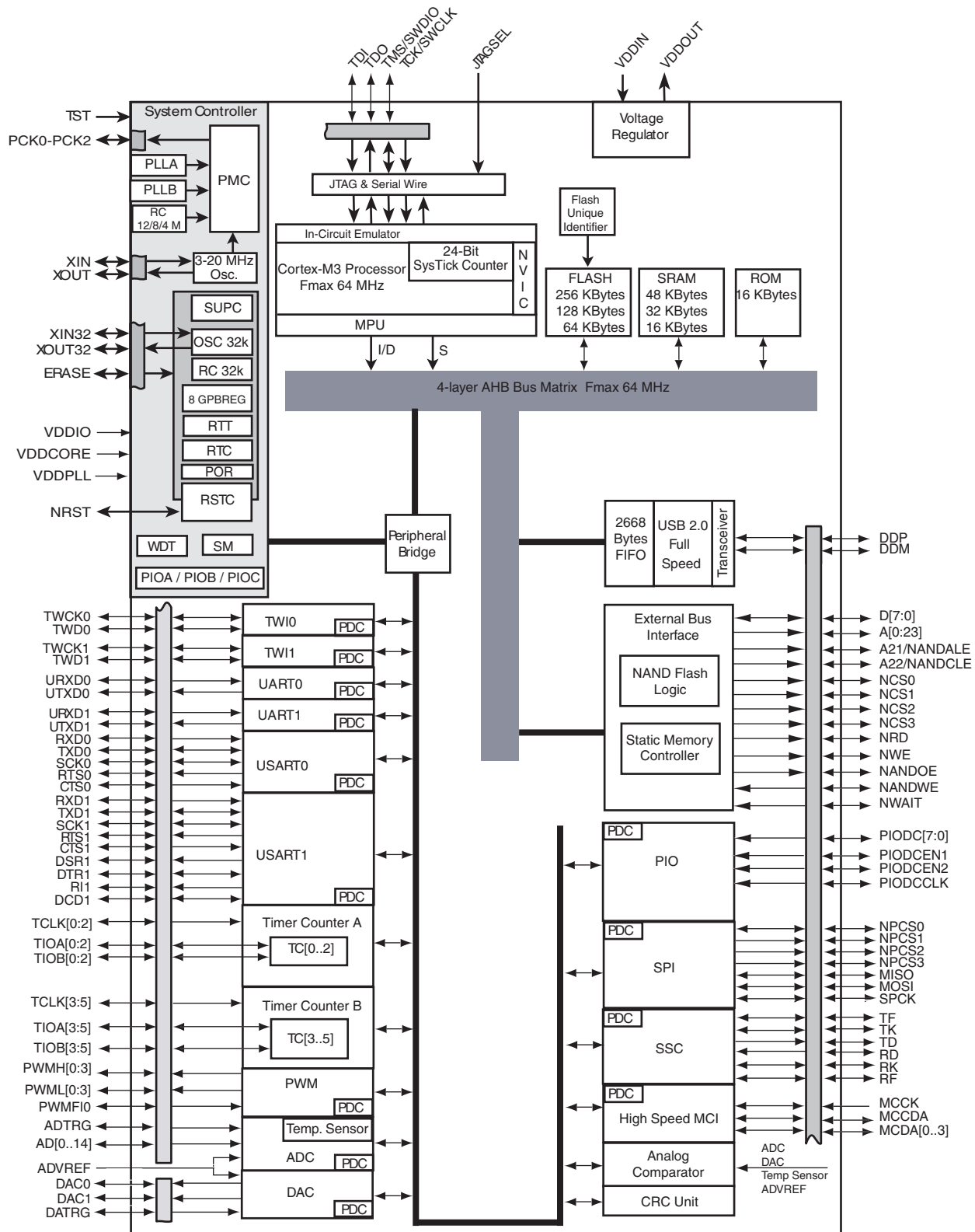


Figure 2-2. SAM3S 64-pin Version Block Diagram

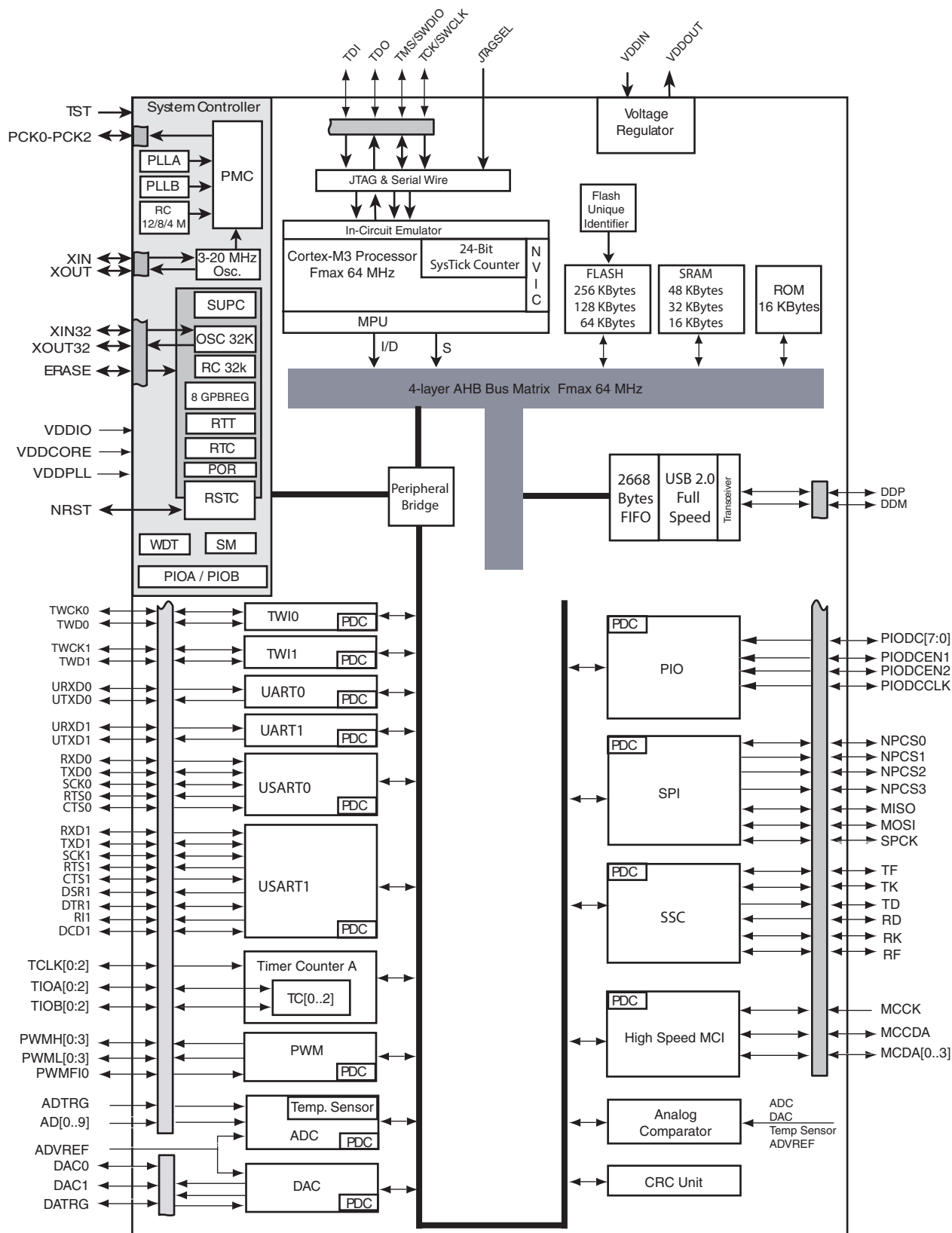
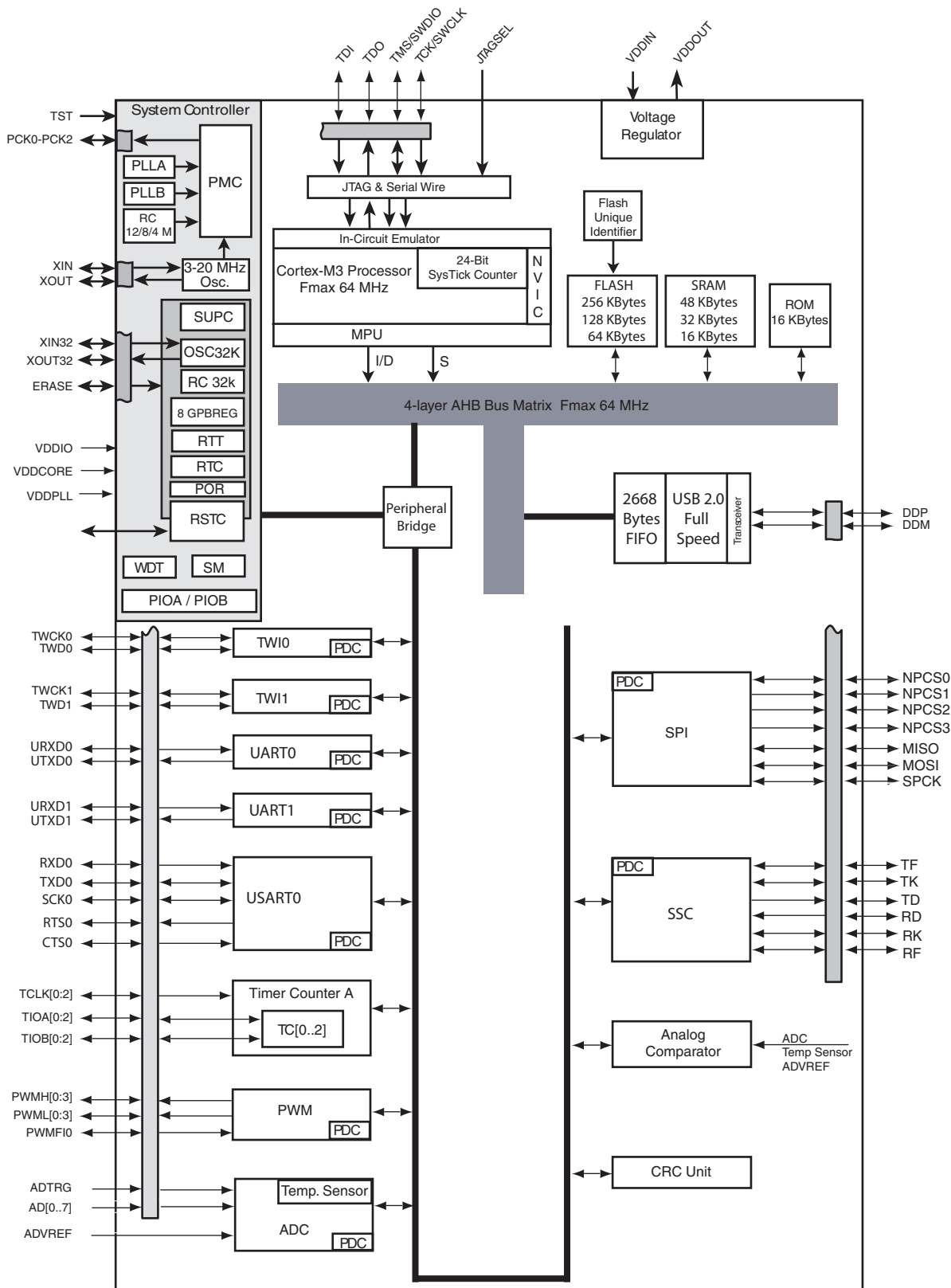


Figure 2-3. SAM3S 48-pin Version Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

| Signal Name | Function | Type | Active Level | Voltage reference | Comments |
|---|--|-------------|--------------|-------------------|---|
| Power Supplies | | | | | |
| VDDIO | Peripherals I/O Lines and USB transceiver Power Supply | Power | | | 1.62V to 3.6V |
| VDDIN | Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply | Power | | | 1.8V to 3.6V ⁽⁴⁾ |
| VDDOUT | Voltage Regulator Output | Power | | | 1.8V Output |
| VDDPLL | Oscillator and PLL Power Supply | Power | | | 1.62 V to 1.95V |
| VDDCORE | Power the core, the embedded memories and the peripherals | Power | | | 1.62V to 1.95V |
| GND | Ground | Ground | | | |
| Clocks, Oscillators and PLLs | | | | | |
| XIN | Main Oscillator Input | Input | | VDDIO | Reset State: - PIO Input - Internal Pull-up disabled - Schmitt Trigger enabled ⁽¹⁾ |
| XOUT | Main Oscillator Output | Output | | | |
| XIN32 | Slow Clock Oscillator Input | Input | | | |
| XOUT32 | Slow Clock Oscillator Output | Output | | | |
| PCK0 - PCK2 | Programmable Clock Output | Output | | | Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled ⁽¹⁾ |
| Serial Wire/JTAG Debug Port - SWJ-DP | | | | | |
| TCK/SWCLK | Test Clock/Serial Wire Clock | Input | | VDDIO | Reset State: - SWJ-DP Mode - Internal pull-up disabled ⁽⁵⁾ - Schmitt Trigger enabled ⁽¹⁾ |
| TDI | Test Data In | Input | | | |
| TDO/TRACESWO | Test Data Out / Trace Asynchronous Data Out | Output | | | |
| TMS/SWDIO | Test Mode Select /Serial Wire Input/Output | Input / I/O | | | |
| JTAGSEL | JTAG Selection | Input | High | | Permanent Internal pull-down |
| Flash Memory | | | | | |
| ERASE | Flash and NVM Configuration Bits Erase Command | Input | High | VDDIO | Reset State: - Erase Input - Internal pull-down enabled - Schmitt Trigger enabled ⁽¹⁾ |
| Reset/Test | | | | | |
| NRST | Synchronous Microcontroller Reset | I/O | Low | VDDIO | Permanent Internal pull-up |
| TST | Test Select | Input | | | Permanent Internal pull-down |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Voltage reference | Comments |
|--|--------------------------------|--------|--------------|-------------------|--|
| Universal Asynchronous Receiver Transmitter - UARTx | | | | | |
| URXDx | UART Receive Data | Input | | | |
| UTXDx | UART Transmit Data | Output | | | |
| PIO Controller - PIOA - PIOB - PIOC | | | | | |
| PA0 - PA31 | Parallel IO Controller A | I/O | | VDDIO | Reset State: - PIO or System IOs ⁽²⁾ - Internal pull-up enabled - Schmitt Trigger enabled ⁽¹⁾ |
| PB0 - PB14 | Parallel IO Controller B | I/O | | | |
| PC0 - PC31 | Parallel IO Controller C | I/O | | | |
| PIO Controller - Parallel Capture Mode (PIOA Only) | | | | | |
| PIODC0-PIODC7 | Parallel Capture Mode Data | Input | | VDDIO | |
| PIODCCCLK | Parallel Capture Mode Clock | Input | | | |
| PIODCEN1-2 | Parallel Capture Mode Enable | Input | | | |
| External Bus Interface | | | | | |
| D0 - D7 | Data Bus | I/O | | | |
| A0 - A23 | Address Bus | Output | | | |
| NWAIT | External Wait Signal | Input | Low | | |
| Static Memory Controller - SMC | | | | | |
| NCS0 - NCS3 | Chip Select Lines | Output | Low | | |
| NRD | Read Signal | Output | Low | | |
| NWE | Write Enable | Output | Low | | |
| NAND Flash Logic | | | | | |
| NANDOE | NAND Flash Output Enable | Output | Low | | |
| NANDWE | NAND Flash Write Enable | Output | Low | | |
| High Speed Multimedia Card Interface - HSMCI | | | | | |
| MCCK | Multimedia Card Clock | I/O | | | |
| MCCDA | Multimedia Card Slot A Command | I/O | | | |
| MCDA0 - MCDA3 | Multimedia Card Slot A Data | I/O | | | |
| Universal Synchronous Asynchronous Receiver Transmitter USARTx | | | | | |
| SCKx | USARTx Serial Clock | I/O | | | |
| TXDx | USARTx Transmit Data | I/O | | | |
| RXDx | USARTx Receive Data | Input | | | |
| RTSx | USARTx Request To Send | Output | | | |
| CTSx | USARTx Clear To Send | Input | | | |
| DTR1 | USART1 Data Terminal Ready | I/O | | | |
| DSR1 | USART1 Data Set Ready | Input | | | |
| DCD1 | USART1 Data Carrier Detect | Input | | | |
| RI1 | USART1 Ring Indicator | Input | | | |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Voltage reference | Comments |
|---|--|-----------------|--------------|-------------------|---|
| Synchronous Serial Controller - SSC | | | | | |
| TD | SSC Transmit Data | Output | | | |
| RD | SSC Receive Data | Input | | | |
| TK | SSC Transmit Clock | I/O | | | |
| RK | SSC Receive Clock | I/O | | | |
| TF | SSC Transmit Frame Sync | I/O | | | |
| RF | SSC Receive Frame Sync | I/O | | | |
| Timer/Counter - TC | | | | | |
| TCLKx | TC Channel x External Clock Input | Input | | | |
| TIOAx | TC Channel x I/O Line A | I/O | | | |
| TIOBx | TC Channel x I/O Line B | I/O | | | |
| Pulse Width Modulation Controller- PWM | | | | | |
| PWMHx | PWM Waveform Output High for channel x | Output | | | |
| PWMLx | PWM Waveform Output Low for channel x | Output | | | only output in complementary mode when dead time insertion is enabled |
| PWMFI0 | PWM Fault Input | Input | | | |
| Serial Peripheral Interface - SPI | | | | | |
| MISO | Master In Slave Out | I/O | | | |
| MOSI | Master Out Slave In | I/O | | | |
| SPCK | SPI Serial Clock | I/O | | | |
| SPI_NPCS0 | SPI Peripheral Chip Select 0 | I/O | Low | | |
| SPI_NPCS1 - SPI_NPCS3 | SPI Peripheral Chip Select | Output | Low | | |
| Two-Wire Interface- TWI | | | | | |
| TWDx | TWlx Two-wire Serial Data | I/O | | | |
| TWCKx | TWlx Two-wire Serial Clock | I/O | | | |
| Analog | | | | | |
| ADVREF | ADC, DAC and Analog Comparator Reference | Analog | | | |
| Analog-to-Digital Converter - ADC | | | | | |
| AD0 - AD14 | Analog Inputs | Analog, Digital | | | |
| ADTRG | ADC Trigger | Input | | VDDIO | |
| 12-bit Digital-to-Analog Converter - DAC | | | | | |
| DAC0 - DAC1 | Analog output | Analog, Digital | | | |
| DACTRG | DAC Trigger | Input | | VDDIO | |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Voltage reference | Comments |
|--|-----------------------|--------------------|--------------|-------------------|---|
| Fast Flash Programming Interface - FFPI | | | | | |
| PGMEN0-PGMEN2 | Programming Enabling | Input | | VDDIO | |
| PGMM0-PGMM3 | Programming Mode | Input | | VDDIO | |
| PGMD0-PGMD15 | Programming Data | I/O | | | |
| PGMRDY | Programming Ready | Output | High | | |
| PGMNVALID | Data Direction | Output | Low | | |
| PGMNOE | Programming Read | Input | Low | | |
| PGMCK | Programming Clock | Input | | | |
| PGMNCMD | Programming Command | Input | Low | | |
| USB Full Speed Device | | | | | |
| DDM | USB Full Speed Data - | Analog, Digital | | VDDIO | Reset State: - USB Mode - Internal Pull-down ⁽³⁾ |
| DDP | USB Full Speed Data + | | | | |

- Notes:
1. Schmitt Triggers can be disabled through PIO registers.
 2. Some PIO lines are shared with System IOs.
 3. Refer to the USB sub section in the product Electrical Characteristics Section for Pull-down value in USB Mode.
 4. See [Section 5.3 “Typical Powering Schematics”](#) for restriction on voltage range of Analog Cells.
 5. TDO pin is set in input mode when the Cortex-M3 Core is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input.

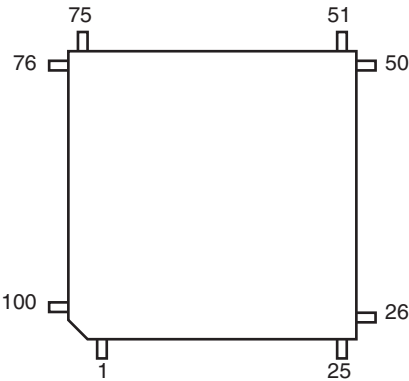
4. Package and Pinout

4.1 SAM3S4/2/1C Package and Pinout

Figure 4-2 shows the orientation of the 100-ball TFBGA Package

4.1.1 100-lead LQFP Package Outline

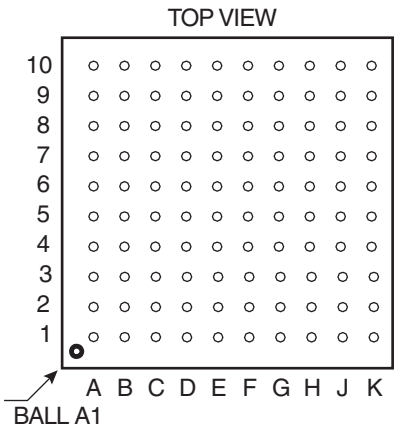
Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball TFBGA Package Outline

The 100-Ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 9 x 9 x 1.1 mm.

Figure 4-2. Orientation of the 100-BALL TFBGA Package



4.1.3 100-Lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3S4/2/1C Pinout

| | | | | | | | |
|----|-----------------|----|---------------------|----|-------------|-----|------------------|
| 1 | ADVREF | 26 | GND | 51 | TDI/PB4 | 76 | TDO/TRACESWO/PB5 |
| 2 | GND | 27 | VDDIO | 52 | PA6/PGMNOE | 77 | JTAGSEL |
| 3 | PB0/AD4 | 28 | PA16/PGMD4 | 53 | PA5/PGMRDY | 78 | PC18 |
| 4 | PC29/AD13 | 29 | PC7 | 54 | PC28 | 79 | TMS/SWDIO/PB6 |
| 5 | PB1/AD5 | 30 | PA15/PGMD3 | 55 | PA4/PGMNCMD | 80 | PC19 |
| 6 | PC30/AD14 | 31 | PA14/PGMD2 | 56 | VDDCORE | 81 | PA31 |
| 7 | PB2/AD6 | 32 | PC6 | 57 | PA27/PGMD15 | 82 | PC20 |
| 8 | PC31 | 33 | PA13/PGMD1 | 58 | PC8 | 83 | TCK/SWCLK/PB7 |
| 9 | PB3/AD7 | 34 | PA24/PGMD12 | 59 | PA28 | 84 | PC21 |
| 10 | VDDIN | 35 | PC5 | 60 | NRST | 85 | VDDCORE |
| 11 | VDDOUT | 36 | VDDCORE | 61 | TST | 86 | PC22 |
| 12 | PA17/PGMD5/AD0 | 37 | PC4 | 62 | PC9 | 87 | ERASE/PB12 |
| 13 | PC26 | 38 | PA25/PGMD13 | 63 | PA29 | 88 | DDM/PB10 |
| 14 | PA18/PGMD6/AD1 | 39 | PA26/PGMD14 | 64 | PA30 | 89 | DDP/PB11 |
| 15 | PA21/PGMD9/AD8 | 40 | PC3 | 65 | PC10 | 90 | PC23 |
| 16 | VDDCORE | 41 | PA12/PGMD0 | 66 | PA3 | 91 | VDDIO |
| 17 | PC27 | 42 | PA11/PGMM3 | 67 | PA2/PGMEN2 | 92 | PC24 |
| 18 | PA19/PGMD7/AD2 | 43 | PC2 | 68 | PC11 | 93 | PB13/DAC0 |
| 19 | PC15/AD11 | 44 | PA10/PGMM2 | 69 | VDDIO | 94 | PC25 |
| 20 | PA22/PGMD10/AD9 | 45 | GND | 70 | GND | 95 | GND |
| 21 | PC13/AD10 | 46 | PA9/PGMM1 | 71 | PC14 | 96 | PB8/XOUT |
| 22 | PA23/PGMD11 | 47 | PC1 | 72 | PA1/PGMEN1 | 97 | PB9/PGMCK/XIN |
| 23 | PC12/AD12 | 48 | PA8/XOUT32/PGMM0 | 73 | PC16 | 98 | VDDIO |
| 24 | PA20/PGMD8/AD3 | 49 | PA7/XIN32/PGMNVALID | 74 | PA0/PGMEN0 | 99 | PB14/DAC1 |
| 25 | PC0 | 50 | VDDIO | 75 | PC17 | 100 | VDDPLL |

4.1.4 100-ball TFBGA Pinout

Table 4-2. 100-ball TFBGA SAM3S4/2/1C Pinout

| | | | | | | | |
|-----|----------------------|-----|----------------|-----|----------------|-----|--------------------------|
| A1 | PB1/AD5 | C6 | TCK/SWCLK/PB7 | F1 | PA18/PGMD6/AD1 | H6 | PC4 |
| A2 | PC29 | C7 | PC16 | F2 | PC26 | H7 | PA11/PGMM3 |
| A3 | VDDIO | C8 | PA1/PGMEN1 | F3 | VDDOUT | H8 | PC1 |
| A4 | PB9/PGMCK/XIN | C9 | PC17 | F4 | GND | H9 | PA6/PGMNOE |
| A5 | PB8/XOUT | C10 | PA0/PGMEN0 | F5 | VDDIO | H10 | TDI/PB4 |
| A6 | PB13/DAC0 | D1 | PB3/AD7 | F6 | PA27/PGMD15 | J1 | PC15/AD11 |
| A7 | DDP/PB11 | D2 | PB0/AD4 | F7 | PC8 | J2 | PC0 |
| A8 | DDM/PB10 | D3 | PC24 | F8 | PA28 | J3 | PA16/PGMD4 |
| A9 | TMS/SWDIO/PB6 | D4 | PC22 | F9 | TST | J4 | PC6 |
| A10 | JTAGSEL | D5 | GND | F10 | PC9 | J5 | PA24/PGMD12 |
| B1 | PC30 | D6 | GND | G1 | PA21/PGMD9/AD8 | J6 | PA25/PGMD13 |
| B2 | ADVREF | D7 | VDDCORE | G2 | PC27 | J7 | PA10/PGMM2 |
| B3 | GNDANA | D8 | PA2/PGMEN2 | G3 | PA15/PGMD3 | J8 | GND |
| B4 | PB14/DAC1 | D9 | PC11 | G4 | VDDCORE | J9 | VDDCORE |
| B5 | PC21 | D10 | PC14 | G5 | VDDCORE | J10 | VDDIO |
| B6 | PC20 | E1 | PA17/PGMD5/AD0 | G6 | PA26/PGMD14 | K1 | PA22/PGMD10/AD9 |
| B7 | PA31 | E2 | PC31 | G7 | PA12/PGMD0 | K2 | PC13/AD10 |
| B8 | PC19 | E3 | VDDIN | G8 | PC28 | K3 | PC12/AD12 |
| B9 | PC18 | E4 | GND | G9 | PA4/PGMNCMD | K4 | PA20/PGMD8/AD3 |
| B10 | TDO/TRACESWO/ PB5 | E5 | GND | G10 | PA5/PGMRDY | K5 | PC5 |
| C1 | PB2/AD6 | E6 | NRST | H1 | PA19/PGMD7/AD2 | K6 | PC3 |
| C2 | VDDPLL | E7 | PA29/AD13 | H2 | PA23/PGMD11 | K7 | PC2 |
| C3 | PC25 | E8 | PA30/AD14 | H3 | PC7 | K8 | PA9/PGMM1 |
| C4 | PC23 | E9 | PC10 | H4 | PA14/PGMD2 | K9 | PA8/XOUT32/PGMM0 |
| C5 | ERASE/PB12 | E10 | PA3 | H5 | PA13/PGMD1 | K10 | PA7/XIN32/ PGMINVALID |

4.2 SAM3S4/2/1B Package and Pinout

Figure 4-3. Orientation of the 64-pad QFN Package

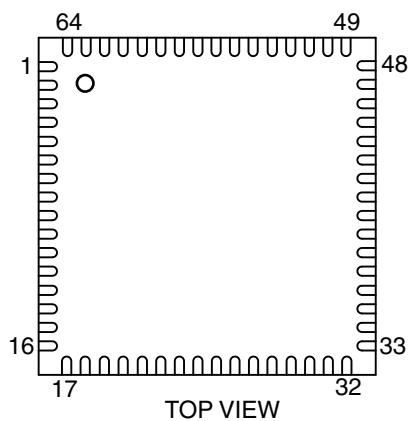
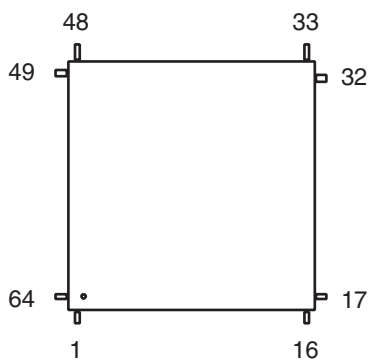


Figure 4-4. Orientation of the 64-lead LQFP Package



4.2.1 64-Lead LQFP and QFN Pinout

64-pin version SAM3S devices are pin-to-pin compatible with AT91SAM7S legacy products. Furthermore, SAM3S products have new functionalities shown in *italic* in [Table 4-3](#).

Table 4-3. 64-pin SAM3S4/2/1B Pinout

| | | | | | | | |
|----|---------------------|----|-------------------------|----|-------------|----|------------------|
| 1 | ADVREF | 17 | GND | 33 | TDI/PB4 | 49 | TDO/TRACESWO/PB5 |
| 2 | GND | 18 | VDDIO | 34 | PA6/PGMNOE | 50 | JTAGSEL |
| 3 | PB0/AD4 | 19 | PA16/PGMD4 | 35 | PA5/PGMRDY | 51 | TMS/SWDIO/PB6 |
| 4 | PB1/AD5 | 20 | PA15/PGMD3 | 36 | PA4/PGMNCMD | 52 | PA31 |
| 5 | PB2/AD6 | 21 | PA14/PGMD2 | 37 | PA27/PGMD15 | 53 | TCK/SWCLK/PB7 |
| 6 | PB3/AD7 | 22 | PA13/PGMD1 | 38 | PA28 | 54 | VDDCORE |
| 7 | VDDIN | 23 | PA24/PGMD12 | 39 | NRST | 55 | ERASE/PB12 |
| 8 | VDDOUT | 24 | VDDCORE | 40 | TST | 56 | DDM/PB10 |
| 9 | PA17/PGMD5/ AD0 | 25 | PA25/PGMD13 | 41 | PA29 | 57 | DDP/PB11 |
| 10 | PA18/PGMD6/ AD1 | 26 | PA26/PGMD14 | 42 | PA30 | 58 | VDDIO |
| 11 | PA21/PGMD9/ AD8 | 27 | PA12/PGMD0 | 43 | PA3 | 59 | PB13/DAC0 |
| 12 | VDDCORE | 28 | PA11/PGMM3 | 44 | PA2/PGMEN2 | 60 | GND |
| 13 | PA19/PGMD7/ AD2 | 29 | PA10/PGMM2 | 45 | VDDIO | 61 | XOUT/PB8 |
| 14 | PA22/PGMD10/ AD9 | 30 | PA9/PGMM1 | 46 | GND | 62 | XIN/PGMCK/PB9 |
| 15 | PA23/PGMD11 | 31 | PA8/XOUT32/ PGMM0 | 47 | PA1/PGMEN1 | 63 | PB14/DAC1 |
| 16 | PA20/PGMD8/ AD3 | 32 | PA7/XIN32/ PGMNVALID | 48 | PA0/PGMEN0 | 64 | VDDPLL |

Note: The bottom pad of the QFN package must be connected to ground.

4.3 SAM3S4/2/1A Package and Pinout

Figure 4-5. Orientation of the 48-pad QFN Package

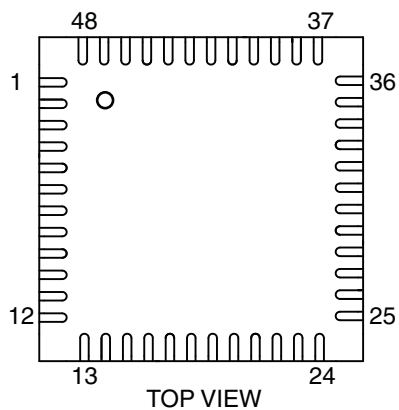
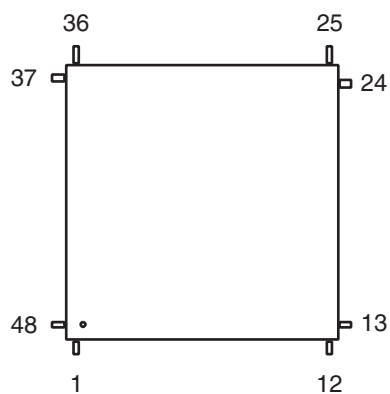


Figure 4-6. Orientation of the 48-lead LQFP Package



4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3S4/2/1A Pinout

| | | | | | | | |
|----|--------------------|----|--------------------------|----|-------------|----|----------------------|
| 1 | ADVREF | 13 | VDDIO | 25 | TDI/PB4 | 37 | TDO/TRACESWO/ PB5 |
| 2 | GND | 14 | PA16/PGMD4 | 26 | PA6/PGMNOE | 38 | JTAGSEL |
| 3 | PB0/AD4 | 15 | PA15/PGMD3 | 27 | PA5/PGMRDY | 39 | TMS/SWDIO/PB6 |
| 4 | PB1/AD5 | 16 | PA14/PGMD2 | 28 | PA4/PGMNCMD | 40 | TCK/SWCLK/PB7 |
| 5 | PB2/AD6 | 17 | PA13/PGMD1 | 29 | NRST | 41 | VDDCORE |
| 6 | PB3/AD7 | 18 | VDDCORE | 30 | TST | 42 | ERASE/PB12 |
| 7 | VDDIN | 19 | PA12/PGMD0 | 31 | PA3 | 43 | DDM/PB10 |
| 8 | VDDOUT | 20 | PA11/PGMM3 | 32 | PA2/PGMEN2 | 44 | DDP/PB11 |
| 9 | PA17/PGMD5/ AD0 | 21 | PA10/PGMM2 | 33 | VDDIO | 45 | XOUT/PB8 |
| 10 | PA18/PGMD6/ AD1 | 22 | PA9/PGMM1 | 34 | GND | 46 | XIN/PB9/PGMCK |
| 11 | PA19/PGMD7/ AD2 | 23 | PA8/XOUT32/ PGMM0 | 35 | PA1/PGMEN1 | 47 | VDDIO |
| 12 | PA20/AD3 | 24 | PA7/XIN32/ PGMINVALID | 36 | PA0/PGMEN0 | 48 | VDDPLL |

Note: The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM3S product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers); USB transceiver; Backup part, 32kHz crystal oscillator and oscillator pads; ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply; Voltage ranges from 1.8V to 3.6V
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator; voltage ranges from 1.62V and 1.95V.

5.2 Voltage Regulator

The SAM3S embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3S. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 μ A static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 μ A.
- In Backup mode, the voltage regulator consumes less than 1 μ A while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 100 μ s.

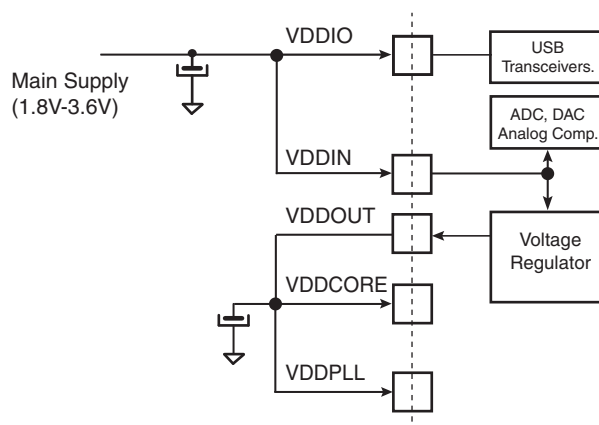
For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM3S supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. [Figure 5-1](#) shows the power schematics.

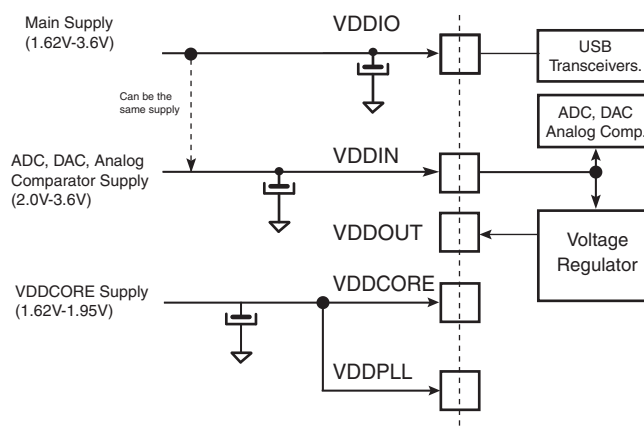
As VDDIN powers the voltage regulator, the ADC/DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

Figure 5-1. Single Supply



Note: For USB, VDDIO needs to be greater than 3.0V.
For ADC, VDDIN needs to be greater than 2.0V.
For DAC, VDDIN needs to be greater than 2.4V.

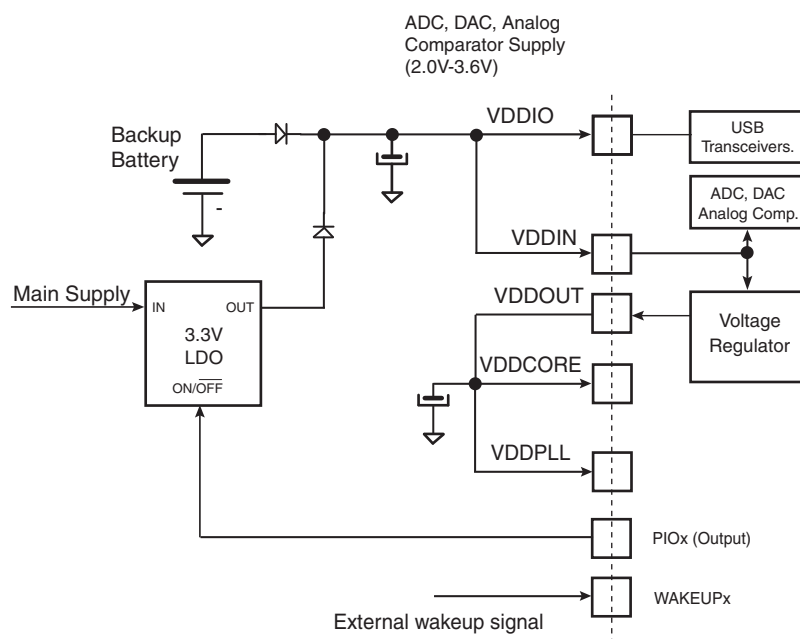
Figure 5-2. Core Externally Supplied



Note: For USB, VDDIO needs to be greater than 3.0V.
 For ADC, VDDIN needs to be greater than 2.0V
 For DAC, VDDIN needs to be greater than 2.4V.

Figure 5-3 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See [Section 5.6 “Wake-up Sources”](#) for further details.

Figure 5-3. Backup Battery



Note: The two diodes provide a “switchover circuit” (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

5.4 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.5 Low Power Modes

The various low power modes of the SAM3S are described below:

5.5.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time ($<0.1\text{ms}$). Total current consumption is $3\text{ }\mu\text{A}$ typical.

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deepsleep mode with the voltage regulator disabled.

The SAM3S can be awakened from this mode through WUP0-15 pins, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode is entered by using WFE instructions with the SLEEPDEEP bit in the System Control Register of the Cortex-M3 set to 1. (See the Power management description in The ARM Cortex M3 Processor section of the product datasheet).

Exit from Backup mode happens if one of the following enable wake up events occurs:

- WKUPEN0-15 pins (level transition, configurable debouncing)
- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than $10\text{ }\mu\text{s}$. Current Consumption in Wait mode is typically $15\text{ }\mu\text{A}$ (total current consumption) if the internal voltage regulator is used or $8\text{ }\mu\text{A}$ if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with $\text{LPM} = 1$ (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WUP0-15 as fast startup wake-up pins (refer to [Section 5.7 "Fast Startup"](#)). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the $4/8/12\text{ MHz}$ fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRSEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSCRSEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

The bit MOSCRSEN should be automatically set to '0'. So you have to add after this instruction the following: while (MOSCRSEN == 0); so that you are sure to stay in the loop until you awake from the wait mode. In that case you are sure the core will not continue to fetch the code but once you have exited the wait mode (in that case MOSCRSEN will be automatically set to '1').

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be woke up from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.5.4 Low Power Mode Summary Table

The modes detailed above are the main low power modes. Each part can be set to on or off separately and wake up sources can be individually configured. [Table 5-1](#) below shows a summary of the configurations of the low power modes.

Table 5-1. Low Power Mode Configuration Summary

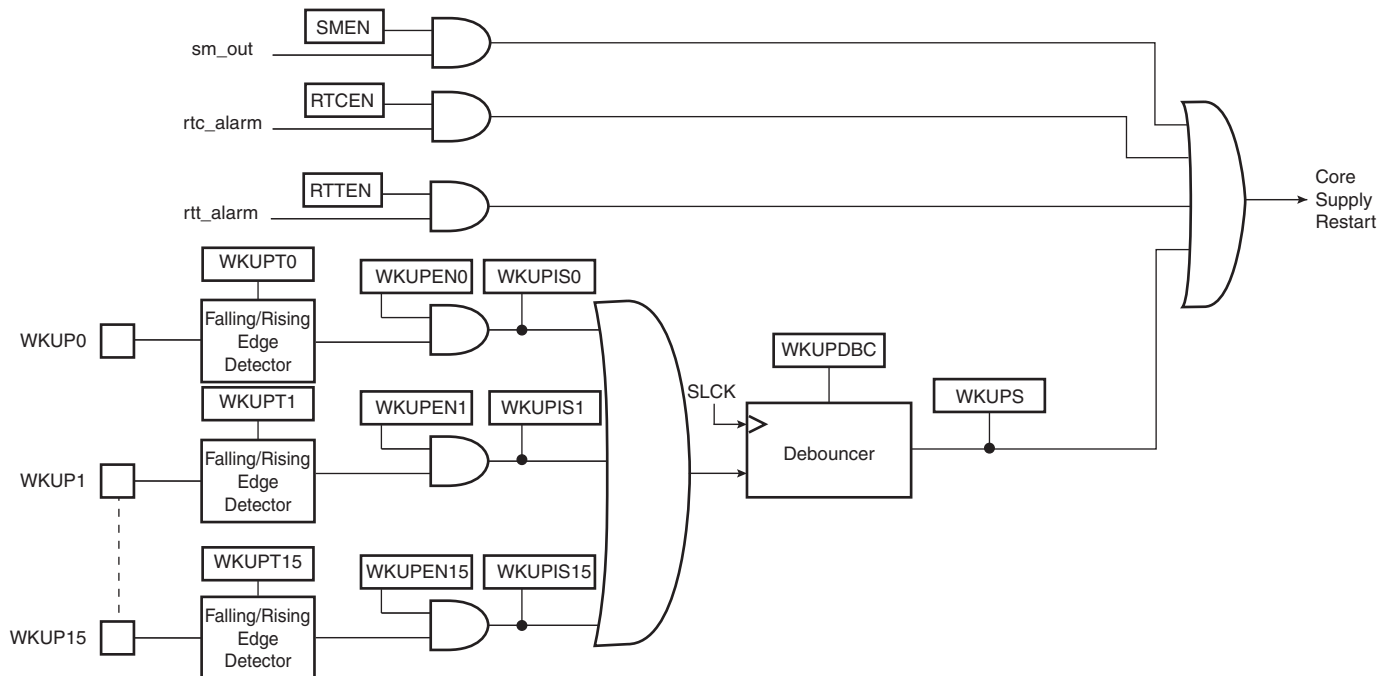
| Mode | SUPC, 32 kHz Oscillator RTC RTT Backup Registers, POR (Backup Region) | Regulator | Core Memory Peripherals | Mode Entry | Potential Wake Up Sources | Core at Wake Up | PIO State while in Low Power Mode | PIO State at Wake Up | Consumption (2) (3) | Wake-up Time ⁽¹⁾ |
|----------------|---|-----------|---|---|---|--------------------|---|---|-------------------------------------|--------------------------------|
| Backup Mode | ON | OFF | OFF (Not powered) | WFE +SLEEPDEEP bit = 1 | WUP0-15 pins SM alarm RTC alarm RTT alarm | Reset | Previous state saved | PIOA & PIOB & PIOC Inputs with pull ups | 3 μ A typ ⁽⁴⁾ | < 0.1 ms |
| Wait Mode | ON | ON | Powered (Not clocked) | WFE +SLEEPDEEP bit = 0 +LPM bit = 1 | Any Event from: Fast startup through WUP0-15 pins RTC alarm RTT alarm USB wake-up | Clocked back | Previous state saved | Unchanged | 5 μ A/15 μ A ⁽⁵⁾ | < 10 μ s |
| Sleep Mode | ON | ON | Powered ⁽⁷⁾ (Not clocked) | WFE or WFI +SLEEPDEEP bit = 0 +LPM bit = 0 | Entry mode =WFI Interrupt Only; Entry mode =WFE Any Enabled Interrupt and/or Any Event from: Fast start-up through WUP0-15 pins RTC alarm RTT alarm USB wake-up | Clocked back | Previous state saved | Unchanged | ⁽⁶⁾ | ⁽⁶⁾ |

- Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
 2. The external loads on PIOs are not taken into account in the calculation.
 3. Supply Monitor current consumption is not included.
 4. Total Current consumption.
 5. 5 μ A on VDDCORE, 15 μ A for total current consumption (using internal voltage regulator), 8 μ A for total current consumption (without using internal voltage regulator).
 6. Depends on MCK frequency.
 7. In this mode the core is supplied and not clocked but some peripherals can be clocked.

5.6 Wake-up Sources

The wake-up events allow the device to exit the backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Source

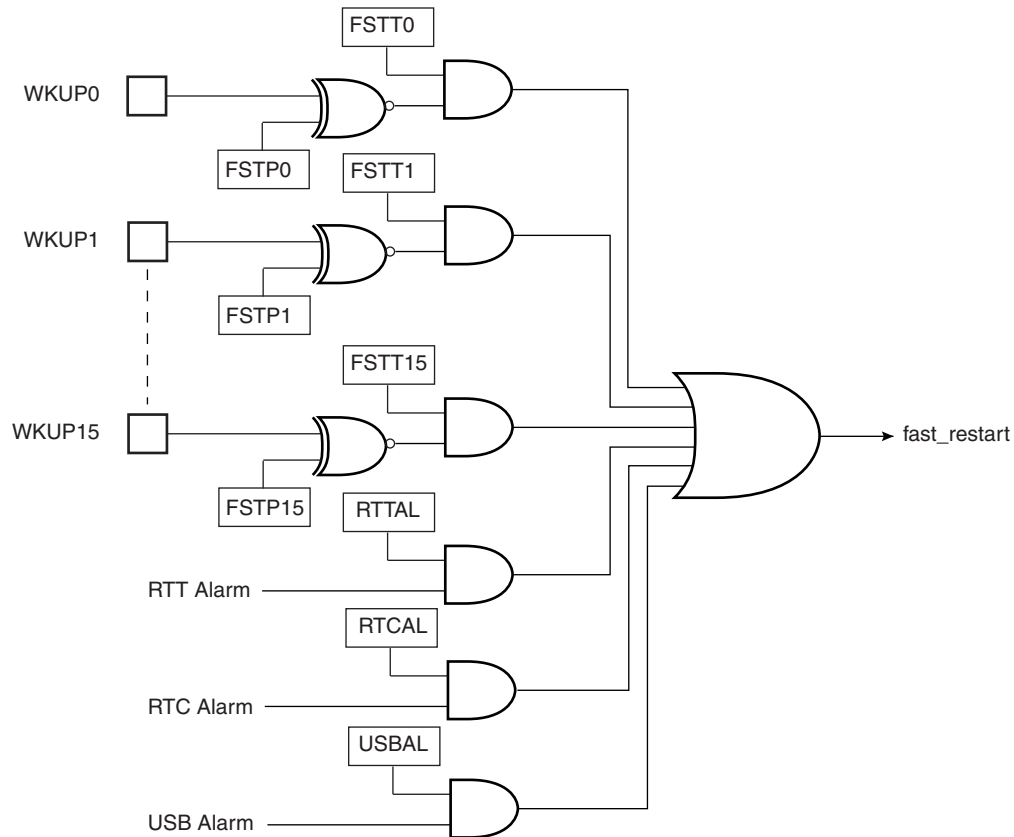


5.7 Fast Startup

The device allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in [Figure 5-5](#), is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4/8/12 MHz fast RC oscillator, switches the master clock on this 4MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Circuitry



6. Input/Output Lines

The SAM3S has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in IO mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

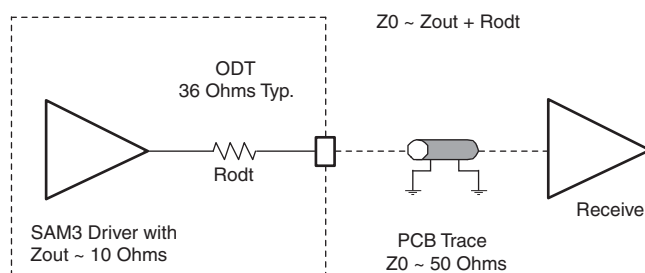
GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to the product PIO controller section.

The input output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM3S embeds high speed pads able to handle up to 32 MHz for HSMCI (MCK/2), 45 MHz for SPI clock lines and 35 MHz on other lines. See AC Characteristics Section in the Electrical Characteristics Section of the datasheet for more details. Typical pull-up and pull-down value is 100 k Ω for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), see [Figure 6-1](#). It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM3S) and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion ODT helps diminish signal integrity issues.

Figure 6-1. On-Die Termination



6.2 System I/O Lines

System I/O lines are pins used by oscillators, test mode, reset and JTAG to name but a few. Described below are the SAM3S system I/O lines shared with PIO lines:

These pins are software configurable as general purpose I/O or system pins. At startup the default function of these pins is always used.

Table 6-1. System I/O Configuration List

| SYSTEM_IO bit number | Default function after reset | Other function | Constraints for normal start | Configuration |
|-------------------------|---------------------------------|----------------|--|---|
| 12 | ERASE | PB12 | Low Level at startup ⁽¹⁾ | In Matrix User Interface Registers (Refer to the SystemIO Configuration Register in the Bus Matrix section of the product datasheet.) |
| 10 | DDM | PB10 | - | |
| 11 | DDP | PB11 | - | |
| 7 | TCK/SWCLK | PB7 | - | |
| 6 | TMS/SWDIO | PB6 | - | |
| 5 | TDO/TRACESWO | PB5 | - | |
| 4 | TDI | PB4 | - | |
| - | PA7 | XIN32 | - | See footnote ⁽²⁾ below |
| - | PA8 | XOUT32 | - | |
| - | PB9 | XIN | - | See footnote ⁽³⁾ below |
| - | PB8 | XOUT | - | |

- Notes:
1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode,
 2. In the product Datasheet Refer to: Slow Clock Generator of the Supply Controller section.
 3. In the product Datasheet Refer to: 3 to 20 MHz Crystal Oscillator information in PMC section.

6.2.1 Serial Wire JTAG Debug Port (SWJ-DP) Pins

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/SWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to [Table 3-1 on page 7](#).

At startup, SWJ-DP pins are configured in SWJ-DP mode to allow connection with debugging probe. Please refer to the Debug and Test Section of the product datasheet.

SWJ-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SWJ-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP. For more information about SW-DP and JTAG-DP switching, please refer to the Debug and Test Section.

6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3S series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length. The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 k Ω . By default, the NRST pin is configured as an input.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 k Ω to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, startup level of this pin must be low to prevent unwanted erasing. Please refer to [Section 11.2 “Peripheral Signal Multiplexing on I/O Lines” on page 41](#). Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store
- Three-stage pipeline
- Single cycle 32-bit multiply
- Hardware divide
- Thumb and Debug states
- Handler and Thread modes
- Low latency ISR entry and exit

7.2 APB/AHB bridge

The SAM3S product embeds one peripheral bridge:

The peripherals of the bridge are clocked by MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3S product manages 4 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

| | |
|----------|---------------------------------|
| Master 0 | Cortex-M3 Instruction/Data |
| Master 1 | Cortex-M3 System |
| Master 2 | Peripheral DMA Controller (PDC) |
| Master 3 | CRC Calculation Unit |

7.4 Matrix Slaves

The Bus Matrix of the SAM3S product manages 5 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

| | |
|---------|------------------------|
| Slave 0 | Internal SRAM |
| Slave 1 | Internal ROM |
| Slave 2 | Internal Flash |
| Slave 3 | External Bus Interface |
| Slave 4 | Peripheral Bridge |

7.5 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the Cortex-M3 S Bus to the Internal ROM. Thus, these paths are forbidden or simply not wired and shown as “-” in the following table.

Table 7-3. SAM3S Master to Slave Access

| Slaves | Masters | 0 | 1 | 2 | 3 |
|--------|------------------------|-------------------|-----------------|-----|-------|
| | | Cortex-M3 I/D Bus | Cortex-M3 S Bus | PDC | CRCCU |
| 0 | Internal SRAM | - | X | X | X |
| 1 | Internal ROM | X | - | X | X |
| 2 | Internal Flash | X | - | - | X |
| 3 | External Bus Interface | - | X | X | X |
| 4 | Peripheral Bridge | - | X | X | - |

7.6 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Low bus arbitration overhead
 - One Master Clock cycle needed for a transfer from memory to peripheral
 - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirement

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 7-4. Peripheral DMA Controller

| Instance Name | Channel T/R | 100 & 64 Pins | 48 Pins |
|---------------|-------------|---------------|---------|
| PWM | Transmit | x | x |
| TWI1 | Transmit | x | x |
| TWI0 | Transmit | x | x |
| UART1 | Transmit | x | x |
| UART0 | Transmit | x | x |
| USART1 | Transmit | x | N/A |
| USART0 | Transmit | x | x |
| DAC | Transmit | x | N/A |
| SPI | Transmit | x | x |
| SSC | Transmit | x | x |
| HSMCI | Transmit | x | N/A |
| PIOA | Transmit | x | x |
| TWI1 | Receive | x | x |
| TWI0 | Receive | x | x |
| UART1 | Receive | x | N/A |
| UART0 | Receive | x | x |

Table 7-4. Peripheral DMA Controller (Continued)

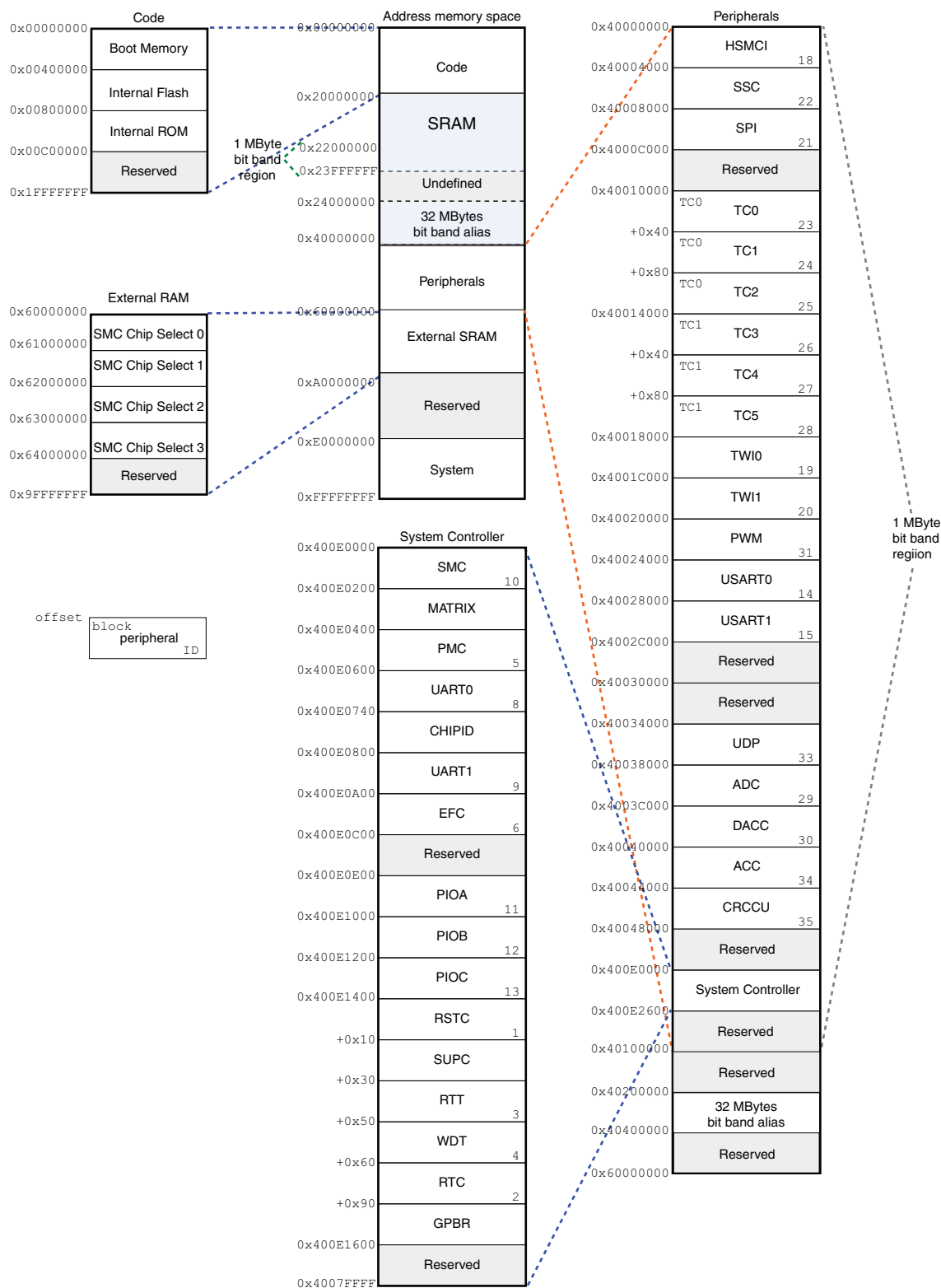
| Instance Name | Channel T/R | 100 & 64 Pins | 48 Pins |
|---------------|-------------|---------------|---------|
| USART1 | Receive | x | x |
| USART0 | Receive | x | x |
| ADC | Receive | x | x |
| SPI | Receive | x | x |
| SSC | Receive | x | x |
| HSMCI | Receive | x | N/A |
| PIOA | Receive | x | x |

7.7 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

8. Product Mapping

Figure 8-1. SAM3S Product Mapping



9. Memories

9.1 Embedded Memories

9.1.1 Internal SRAM

The ATSAM3S4 product (256-Kbyte internal Flash version) embeds a total of 48 Kbytes high-speed SRAM.

The ATSAM3S2 product (128-Kbyte internal Flash version) embeds a total of 32 Kbytes high-speed SRAM.

The ATSAM3S1 product (64-Kbyte internal Flash version) embeds a total of 16 Kbytes high-speed SRAM.

The SRAM is accessible over System Cortex-M3 bus at address 0x2000 0000.

The SRAM is in the bit band region. The bit band alias region is mapped from 0x2200 0000 to 0x23FF FFFF.

9.1.2 Internal ROM

The SAM3S product embeds an Internal ROM, which contains the SAM Boot Assistant (SAM-BA), In Application Programming routines (IAP) and Fast Flash Programming Interface (FFPI).

At any time, the ROM is mapped at address 0x0080 0000.

9.1.3 Embedded Flash

9.1.3.1 Flash Overview

The Flash of the ATSAM3S4 (256-Kbytes internal Flash version) is organized in one bank of 1024 pages (Single plane) of 256 bytes.

The Flash of the ATSAM3S2 (128-Kbytes internal Flash version) is organized in one bank of 512 pages (Single plane) of 256 bytes.

The Flash of the ATSAM3S1 (64-Kbytes internal Flash version) is organized in one bank of 256 pages (Single plane) of 256 bytes.

The Flash contains a 128-byte write buffer, accessible through a 32-bit interface.

9.1.3.2 Flash Power Supply

The Flash is supplied by VDDCORE.

9.1.3.3 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller (EEFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped on the APB.

The Enhanced Embedded Flash Controller ensures the interface of the Flash block with the 32-bit internal bus. Its 128-bit wide memory interface increases performance.

The user can choose between high performance or lower current consumption by selecting either 128-bit or 64-bit access. It also manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.

One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic.

9.1.3.4 Flash Speed

The user needs to set the number of wait states depending on the frequency used.

For more details, refer to the AC Characteristics sub section in the product Electrical Characteristics Section.

9.1.3.5 Lock Regions

Several lock bits used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. Number of Lock Bits

| Product | Number of Lock Bits | Lock Region Size |
|----------|---------------------|----------------------|
| ATSAM3S4 | 16 | 16 kbytes (64 pages) |
| ATSAM3S2 | 8 | 16 kbytes (64 pages) |
| ATSAM3S1 | 4 | 16 kbytes (64 pages) |

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.6 Security Bit Feature

The SAM3S features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, SRAM, Core Registers and Internal Peripherals either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command "Set General Purpose NVM Bit 0" of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core registers, Internal Peripherals are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.7 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.8 Unique Identifier

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

9.1.3.9 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST is tied high and PA0 and PA1 are tied low.

9.1.3.10 SAM-BA[®] Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

9.1.3.11 GPNVM Bits

The SAM3S features two GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

Table 9-2. General Purpose Non-volatile Memory Bits

| GPNVMBit[#] | Function |
|-------------|---------------------|
| 0 | Security bit |
| 1 | Boot mode selection |

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general-purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

9.2 External Memories

The SAM3S features an External Bus Interface to provide the interface to a wide range of external memories and to any parallel peripheral.

9.2.1 Static Memory Controller

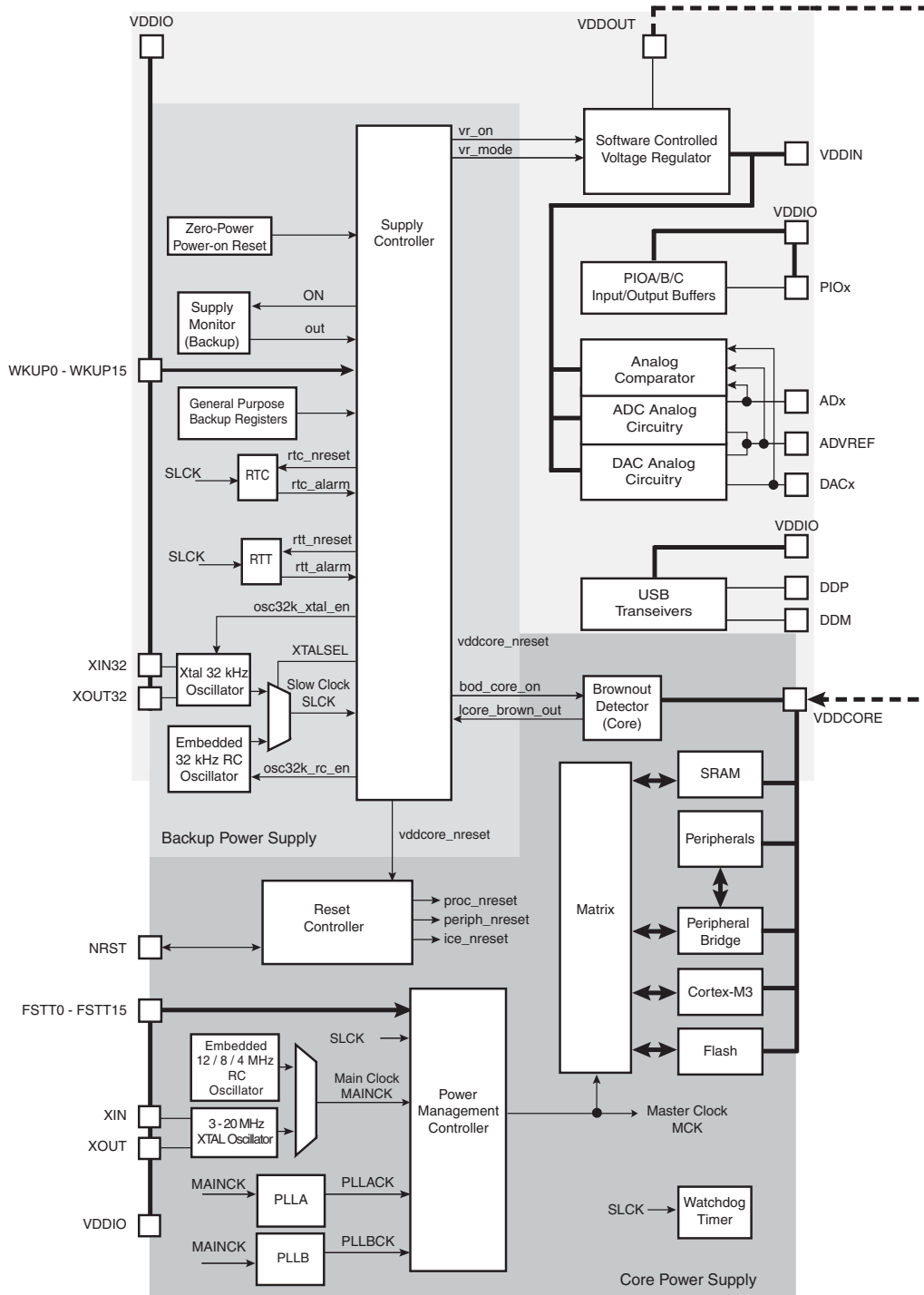
- 8-bit Data Bus
- Up to 24-bit Address Bus (up to 16 MBytes linear per chip select)
- Up to 4 chip selects, Configurable Assignment
- Multiple Access Modes supported
 - Chip Select, Write enable or Read enable Control Mode
 - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
 - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
 - Programmable Wait State Generation
 - External Wait Request
 - Programmable Data Float Time
- Slow Clock mode supported
- Additional Logic for NAND Flash

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the system controller block diagram in [Figure 10-1 on page 34](#).

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

10.1 System Controller and Peripheral Mapping

Please refer to [Section 8-1 “SAM3S Product Mapping” on page 30](#).

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on-Reset, Brownout and Supply Monitor

The SAM3S embeds three features to monitor, warn and/or reset the chip:

- Power-on-Reset on VDDIO
- Brownout Detector on VDDCORE
- Supply Monitor on VDDIO

10.2.1 Power-on-Reset

The Power-on-Reset monitors VDDIO. It is always activated and monitors voltage at start up but also during power down. If VDDIO goes below the threshold voltage, the entire chip is reset. For more information, refer to the Electrical Characteristics section of the datasheet.

10.2.2 Brownout Detector on VDDCORE

The Brownout Detector monitors VDDCORE. It is active by default. It can be deactivated by software through the Supply Controller (SUPC_MR). It is especially recommended to disable it during low-power modes such as wait or sleep modes. If VDDCORE goes below the threshold voltage, the reset of the core is asserted. For more information, refer to the Supply Controller (SUPC) and Electrical Characteristics sections of the datasheet.

10.2.3 Supply Monitor on VDDIO

The Supply Monitor monitors VDDIO. It is not active by default. It can be activated by software and is fully programmable with 16 steps for the threshold (between 1.9V to 3.4V). It is controlled by the Supply Controller (SUPC). A sample mode is possible. It allows to divide the supply monitor power consumption by a factor of up to 2048. For more information, refer to the SUPC and Electrical Characteristics sections of the datasheet.

10.3 Reset Controller

The Reset Controller is based on a Power-on-Reset cell, and a Supply Monitor on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset, a wake-up reset, a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin input/output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDIO.

10.4 Supply Controller (SUPC)

The Supply Controller controls the power supplies of each section of the processor and the peripherals (via Voltage regulator control)

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz Slow clock generator.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

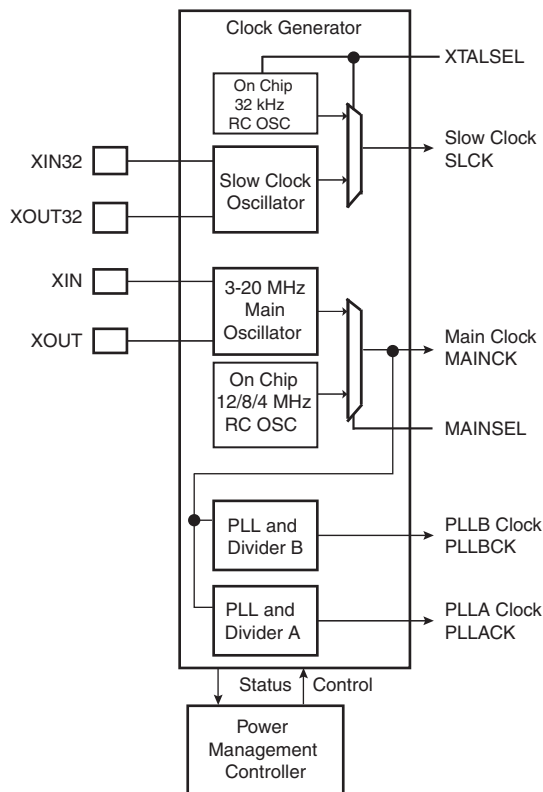
It also enables to set the system in different low power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768Hz Slow Clock oscillator with bypass mode
- One Low-Power RC oscillator
- One 3-20 MHz Crystal Oscillator, which can be bypassed
- One Fast RC oscillator factory programmed, 3 output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 60 to 130 MHz PLL (PLL B) providing a clock for the USB Full Speed Controller
- One 60 to 130 MHz programmable PLL (PLL A), capable to provide the clock MCK to the processor and to the peripherals. The PLLA input frequency is from 3.5 to 20 MHz.

Figure 10-2. Clock Generator Block Diagram



10.6 Power Management Controller

The Power Management Controller provides all the clock signals to the system. It provides:

- the Processor Clock, HCLK
- the Free running processor clock, FCLK
- the Cortex SysTick external clock
- the Master Clock, MCK, in particular to the Matrix and the memory interfaces
- the USB Clock, UDPCCK

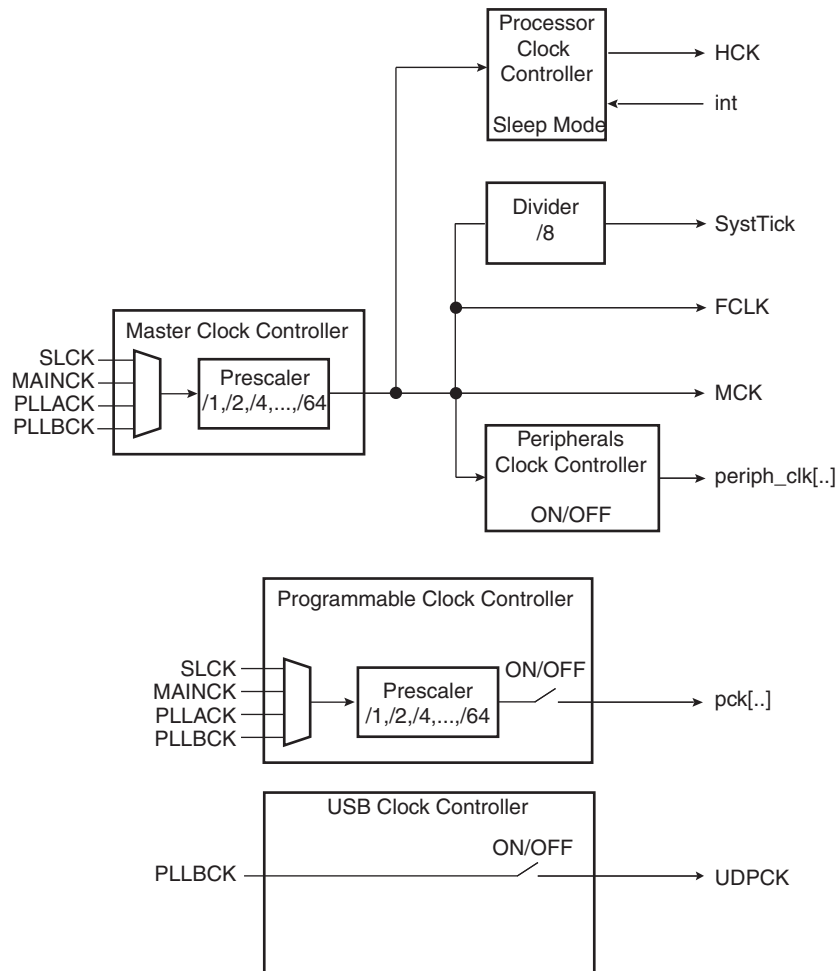
- independent peripheral clocks, typically at the frequency of MCK
- three programmable clock outputs: PCK0, PCK1 and PCK2

The Supply Controller selects between the 32 kHz RC oscillator or the crystal oscillator. The unused oscillator is disabled automatically so that power consumption is optimized.

By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 4 MHz.

The user can trim the 8 and 12 MHz RC Oscillator frequency by software.

Figure 10-3. SAM3S Power Management Controller Block Diagram



The SysTick calibration value is fixed at 8000 which allows the generation of a time base of 1 ms with SysTick clock at 8 MHz (max HCLK/8 = 64 MHz/8).

10.7 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access.

10.8 SysTick Timer

- 24-bit down counter
- Self-reload capability
- Flexible System timer

10.9 Real Time Timer

- Real Time Timer, allowing backup of time with different accuracies
 - 32-bit free-running back-up counter
 - Integrates a 16-bit programmable prescaler running on slow clock
 - Alarm register capable to generate a wake-up of the system through the Shut Down Controller

10.10 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

10.11 General Purpose Backup Registers

- Eight 32-bit general-purpose backup registers

10.12 Nested Vectored Interrupt Controller

- Thirty maskable external interrupts
- Sixteen priority levels
- Processor state automatically saved on interrupt entry, and restored on
- Dynamic reprioritization of interrupts
- Priority grouping.
 - selection of preempting interrupt levels and non-preempting interrupt levels.
- Support for tail-chaining and late arrival of interrupts.
 - back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

10.13 Chip Identification

- Chip Identifier (CHIPID) registers permit recognition of the device and its revision.

Table 10-1. SAM3S Chip IDs Register

| Chip Name | Flash Size (KBytes) | Pin Count | DBGU_CIDR | CHIPID_EXID |
|-------------------|---------------------|-----------|------------|-------------|
| ATSAM3S4A (Rev A) | 256 | 48 | 0x28800960 | 0x0 |
| ATSAM3S2A (Rev A) | 128 | 48 | 0x288A0760 | 0x0 |
| ATSAM3S1A (Rev A) | 64 | 48 | 0x28890560 | 0x0 |
| ATSAM3S4B (Rev A) | 256 | 64 | 0x28900960 | 0x0 |
| ATSAM3S2B (Rev A) | 128 | 64 | 0x289A0760 | 0x0 |
| ATSAM3S1B (Rev A) | 64 | 64 | 0x28990560 | 0x0 |
| ATSAM3S4C (Rev A) | 256 | 100 | 0x28A00960 | 0x0 |
| ATSAM3S2C (Rev A) | 128 | 100 | 0x28AA0760 | 0x0 |
| ATSAM3S1C (Rev A) | 64 | 100 | 0x28A90560 | 0x0 |

- JTAG ID: 0x05B2D03F

10.14 UART

- Two-pin UART
 - Implemented features are 100% compatible with the standard Atmel USART
 - Independent receiver and transmitter with a common programmable Baud Rate Generator
 - Even, Odd, Mark or Space Parity Generation
 - Parity, Framing and Overrun Error Detection
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
 - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. PIO available according to pin count

| Version | 48 pin | 64 pin | 100 pin |
|---------|--------|--------|---------|
| PIOA | 21 | 32 | 32 |
| PIOB | 13 | 15 | 15 |
| PIOC | - | - | 32 |

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
 - Input change, rising edge, falling edge, low level and level interrupt
 - Debouncing and Glitch filter
 - Multi-drive option enables driving in open drain
 - Programmable pull-up or pull-down on each I/O line
 - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3S. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 11-1. Peripheral Identifiers

| Instance ID | Instance Name | NVIC Interrupt | PMC Clock Control | Instance Description |
|-------------|---------------|----------------|-------------------|--------------------------------------|
| 0 | SUPC | X | | Supply Controller |
| 1 | RSTC | X | | Reset Controller |
| 2 | RTC | X | | Real Time Clock |
| 3 | RTT | X | | Real Time Timer |
| 4 | WDT | X | | Watchdog Timer |
| 5 | PMC | X | | Power Management Controller |
| 6 | EEFC | X | | Enhanced Embedded Flash Controller |
| 7 | - | - | | Reserved |
| 8 | UART0 | X | X | UART 0 |
| 9 | UART1 | X | X | UART 1 |
| 10 | SMC | X | X | SMC |
| 11 | PIOA | X | X | Parallel I/O Controller A |
| 12 | PIOB | X | X | Parallel I/O Controller B |
| 13 | PIOC | X | X | Parallel I/O Controller C |
| 14 | USART0 | X | X | USART 0 |
| 15 | USART1 | X | X | USART 1 |
| 16 | - | - | - | Reserved |
| 17 | - | - | - | Reserved |
| 18 | HSMCI | X | X | High Speed Multimedia Card Interface |
| 19 | TWI0 | X | X | Two Wire Interface 0 |
| 20 | TWI1 | X | X | Two Wire Interface 1 |
| 21 | SPI | X | X | Serial Peripheral Interface |
| 22 | SSC | X | X | Synchronous Serial Controller |
| 23 | TC0 | X | X | Timer/Counter 0 |
| 24 | TC1 | X | X | Timer/Counter 1 |
| 25 | TC2 | X | X | Timer/Counter 2 |
| 26 | TC3 | X | X | Timer/Counter 3 |
| 27 | TC4 | X | X | Timer/Counter 4 |
| 28 | TC5 | X | X | Timer/Counter 5 |
| 29 | ADC | X | X | Analog-to-Digital Converter |
| 30 | DACC | X | X | Digital-to-Analog Converter |
| 31 | PWM | X | X | Pulse Width Modulation |
| 32 | CRCCU | X | X | CRC Calculation Unit |
| 33 | ACC | X | X | Analog Comparator |
| 34 | UDP | X | X | USB Device Port |

11.2 Peripheral Signal Multiplexing on I/O Lines

The SAM3S product features 2 PIO controllers on 48-pin and 64-pin versions (PIOA, PIOB) or 3 PIO controllers on the 100-pin version, (PIOA, PIOB, PIOC), that multiplex the I/O lines of the peripheral set.

The SAM3S 64-pin and 100-pin PIO Controllers control up to 32 lines. (See, [Table 10-2](#).) Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following pages define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

11.2.1 PIO Controller A Multiplexing

Table 11-2. Multiplexing on PIO Controller A (PIOA)

| I/O Line | Peripheral A | Peripheral B | Peripheral C | Extra Function | System Function | Comments |
|----------|--------------|--------------|--------------|-----------------|-----------------|---------------------|
| PA0 | PWMH0 | TIOA0 | A17 | WKUP0 | | High drive |
| PA1 | PWMH1 | TIOB0 | A18 | WKUP1 | | High drive |
| PA2 | PWMH2 | SCK0 | DATRG | WKUP2 | | High drive |
| PA3 | TWD0 | NPCS3 | | | | High drive |
| PA4 | TWCK0 | TCLK0 | | WKUP3 | | |
| PA5 | RXD0 | NPCS3 | | WKUP4 | | |
| PA6 | TXD0 | PCK0 | | | | |
| PA7 | RTS0 | PWMH3 | | | XIN32 | |
| PA8 | CTS0 | ADTRG | | WKUP5 | XOUT32 | |
| PA9 | URXD0 | NPCS1 | PWMFI0 | WKUP6 | | |
| PA10 | UTXD0 | NPCS2 | | | | |
| PA11 | NPCS0 | PWMH0 | | WKUP7 | | |
| PA12 | MISO | PWMH1 | | | | |
| PA13 | MOSI | PWMH2 | | | | |
| PA14 | SPCK | PWMH3 | | WKUP8 | | |
| PA15 | TF | TIOA1 | PWML3 | WKUP14/PIODCEN1 | | |
| PA16 | TK | TIOB1 | PWML2 | WKUP15/PIODCEN2 | | |
| PA17 | TD | PCK1 | PWMH3 | AD0 | | |
| PA18 | RD | PCK2 | A14 | AD1 | | |
| PA19 | RK | PWML0 | A15 | AD2/WKUP9 | | |
| PA20 | RF | PWML1 | A16 | AD3/WKUP10 | | |
| PA21 | RXD1 | PCK1 | | AD8 | | 64/100-pin versions |
| PA22 | TXD1 | NPCS3 | NCS2 | AD9 | | 64/100-pin versions |
| PA23 | SCK1 | PWMH0 | A19 | PIODCCLK | | 64/100-pin versions |
| PA24 | RTS1 | PWMH1 | A20 | PIODC0 | | 64/100-pin versions |
| PA25 | CTS1 | PWMH2 | A23 | PIODC1 | | 64/100-pin versions |
| PA26 | DCD1 | TIOA2 | MCDA2 | PIODC2 | | 64/100-pin versions |
| PA27 | DTR1 | TIOB2 | MCDA3 | PIODC3 | | 64/100-pin versions |
| PA28 | DSR1 | TCLK1 | MCCDA | PIODC4 | | 64/100-pin versions |
| PA29 | RI1 | TCLK2 | MCCK | PIODC5 | | 64/100-pin versions |
| PA30 | PWML2 | NPCS2 | MCDA0 | WKUP11/PIODC6 | | 64/100-pin versions |
| PA31 | NPCS1 | PCK2 | MCDA1 | PIODC7 | | 64/100-pin versions |

11.2.2 PIO Controller B Multiplexing

Table 11-3. Multiplexing on PIO Controller B (PIOB)

| I/O Line | Peripheral A | Peripheral B | Peripheral C | Extra Function | System Function | Comments |
|----------|--------------|--------------|--------------|----------------|-----------------|---------------------|
| PB0 | PWMH0 | | | AD4 | | |
| PB1 | PWMH1 | | | AD5 | | |
| PB2 | URXD1 | NPCS2 | | AD6/ WKUP12 | | |
| PB3 | UTXD1 | PCK2 | | AD7 | | |
| PB4 | TWD1 | PWMH2 | | | TDI | |
| PB5 | TWCK1 | PWML0 | | WKUP13 | TDO/TRACESWO | |
| PB6 | | | | | TMS/SWDIO | |
| PB7 | | | | | TCK/SWCLK | |
| PB8 | | | | | XOUT | |
| PB9 | | | | | XIN | |
| PB10 | | | | | DDM | |
| PB11 | | | | | DDP | |
| PB12 | PWML1 | | | | ERASE | |
| PB13 | PWML2 | PCK0 | | DAC0 | | 64/100-pin versions |
| PB14 | NPCS1 | PWMH3 | | DAC1 | | 64/100-pin versions |

11.2.3 PIO Controller C Multiplexing

Table 11-4. Multiplexing on PIO Controller C (PIOC)

| I/O Line | Peripheral A | Peripheral B | Peripheral C | Extra Function | System Function | Comments |
|----------|--------------|--------------|--------------|----------------|-----------------|-----------------|
| PC0 | D0 | PWML0 | | | | 100-pin version |
| PC1 | D1 | PWML1 | | | | 100-pin version |
| PC2 | D2 | PWML2 | | | | 100-pin version |
| PC3 | D3 | PWML3 | | | | 100-pin version |
| PC4 | D4 | NPCS1 | | | | 100-pin version |
| PC5 | D5 | | | | | 100-pin version |
| PC6 | D6 | | | | | 100-pin version |
| PC7 | D7 | | | | | 100-pin version |
| PC8 | NWE | | | | | 100-pin version |
| PC9 | NANDOE | | | | | 100-pin version |
| PC10 | NANDWE | | | | | 100-pin version |
| PC11 | NRD | | | | | 100-pin version |
| PC12 | NCS3 | | | AD12 | | 100-pin version |
| PC13 | NWAIT | PWML0 | | AD10 | | 100-pin version |
| PC14 | NCS0 | | | | | 100-pin version |
| PC15 | NCS1 | PWML1 | | AD11 | | 100-pin version |
| PC16 | A21/NANDALE | | | | | 100-pin version |
| PC17 | A22/NANDCLE | | | | | 100-pin version |
| PC18 | A0 | PWMH0 | | | | 100-pin version |
| PC19 | A1 | PWMH1 | | | | 100-pin version |
| PC20 | A2 | PWMH2 | | | | 100-pin version |
| PC21 | A3 | PWMH3 | | | | 100-pin version |
| PC22 | A4 | PWML3 | | | | 100-pin version |
| PC23 | A5 | TIOA3 | | | | 100-pin version |
| PC24 | A6 | TIOB3 | | | | 100-pin version |
| PC25 | A7 | TCLK3 | | | | 100-pin version |
| PC26 | A8 | TIOA4 | | | | 100-pin version |
| PC27 | A9 | TIOB4 | | | | 100-pin version |
| PC28 | A10 | TCLK4 | | | | 100-pin version |
| PC29 | A11 | TIOA5 | | AD13 | | 100-pin version |
| PC30 | A12 | TIOB5 | | AD14 | | 100-pin version |
| PC31 | A13 | TCLK5 | | | | 100-pin version |

12. Embedded Peripherals Overview

12.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
 - Four chip selects with external decoder support allow communication with up to 15 peripherals
 - Serial memories, such as DataFlash and 3-wire EEPROMs
 - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
 - External co-processors
- Master or slave serial peripheral bus interface
 - 8- to 16-bit programmable data length per chip select
 - Programmable phase and polarity per chip select
 - Programmable transfer delays between consecutive transfers and between clock and data per chip select
 - Programmable delay between consecutive transfers
 - Selectable mode fault detection
- Very fast transfers supported
 - Transfers with baud rates up to MCK
 - The chip select line may be left active to speed up transfers on the same device

12.2 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- Compatibility with Atmel two-wire interface, serial memory and I²C compatible devices
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 kbit/s
- General Call Supported in Slave Mode
- Connecting to PDC channel capabilities optimizes data transfers in Master Mode only
 - One channel for the receiver, one channel for the transmitter
 - Next buffer support

12.3 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
 - Independent receiver and transmitter with a common programmable Baud Rate Generator
 - Even, Odd, Mark or Space Parity Generation
 - Parity, Framing and Overrun Error Detection
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
 - Support for two PDC channels with connection to receiver and transmitter

12.4 Universal Synchronous Asynchronous Receiver Transceiver (USART)

- Programmable Baud Rate Generator with Fractional Baud rate support
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
 - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
 - Parity generation and error detection
 - Framing error detection, overrun error detection
 - MSB- or LSB-first
 - Optional break generation and detection

- By 8 or by-16 over-sampling receiver frequency
- Hardware handshaking RTS-CTS
- Receiver time-out and transmitter timeguard
- Optional Multi-drop Mode with address generation and detection
- Optional Manchester Encoding
- Full modem line support on USART1 (DCD-DSR-DTR-R1)
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
 - NACK handling, error counter with repetition and iteration limit
- SPI Mode
 - Master or Slave
 - Serial Clock programmable Phase and Polarity
 - SPI Serial Clock (SCK) Frequency up to MCK/4
- IrDA modulation and demodulation
 - Communication at up to 115.2 Kbps
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo

12.5 Synchronous Serial Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I²S, TDM Buses, Magnetic Card Reader)
- Contains an independent receiver and transmitter and a common clock divider
- Offers configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

12.6 Timer Counter (TC)

- Six 16-bit Timer Counter Channels
- Wide range of functions including:
 - Frequency Measurement
 - Event Counting
 - Interval Measurement
 - Pulse Generation
 - Delay Timing
 - Pulse Width Modulation
 - Up/down Capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs
 - Five internal clock inputs
 - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
 - Advanced line filtering
 - Position / revolution / speed
- 2-bit Gray Up/Down Counter for Stepper Motor

12.7 Pulse Width Modulation Controller (PWM)

- One Four-channel 16-bit PWM Controller, 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
 - A Modulo n counter providing eleven clocks
 - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
 - Independent Enable Disable Commands
 - Independent Clock Selection
 - Independent Period and Duty Cycle, with Double Buffering
 - Programmable selection of the output waveform polarity
 - Programmable center or left aligned output waveform
 - Independent Output Override for each channel
 - Independent complementary Outputs with 12-bit dead time generator for each channel
 - Independent Enable Disable Commands
 - Independent Clock Selection
 - Independent Period and Duty Cycle, with Double Buffering
- Synchronous Channel mode
 - Synchronous Channels share the same counter
 - Mode to update the synchronous channels registers after a programmable number of periods
- Connection to one PDC channel
 - Offers Buffer transfer without Processor Intervention, to update duty cycle of synchronous channels
- independent event lines which can send up to 4 triggers on ADC within a period
- Programmable Fault Input providing an asynchronous protection of outputs
- Stepper motor control (2 Channels)

12.8 High Speed Multimedia Card Interface (HSMCI)

- 4-bit or 1-bit Interface
- Compatibility with MultiMedia Card Specification Version 4.3
- Compatibility with SD and SDHC Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V1.1.
- Compatibility with CE-ATA Specification 1.1
- Cards clock rate up to Master Clock divided by 2
- Boot Operation Mode support
- High Speed mode support
- Embedded power management to slow down clock rate when not used
- HSMCI has one slot supporting
 - One MultiMediaCard bus (up to 30 cards) or
 - One SD Memory Card
 - One SDIO Card
- Support for stream, block and multi-block data read and write

12.9 USB Device Port (UDP)

- USB V2.0 full-speed compliant, 12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints

- Eight endpoints
 - Endpoint 0: 64 bytes
 - Endpoint 1 and 2: 64 bytes ping-pong
 - Endpoint 3: 64 bytes
 - Endpoint 4 and 5: 512 bytes ping-pong
 - Endpoint 6 and 7: 64 bytes ping-pong
 - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP
- Pull-down resistor on DDM and DDP when disabled

12.10 Analog-to-Digital Converter (ADC)

- up to 16 Channels,
- 10/12-bit resolution
- up to 1 MSample/s
- programmable sequence of conversion on each channel
- Integrated temperature sensor
- Single ended/differential conversion
- Programmable gain: 1, 2, 4

12.11 Digital-to-Analog Converter (DAC)

- Up to 2 channel 12-bit DAC
- Up to 2 mega-samples conversion rate in single channel mode
- Flexible conversion range
- Multiple trigger sources for each channel
- 2 Sample/Hold (S/H) outputs
- Built-in offset and gain calibration
- Possibility to drive output to ground
- Possibility to use as input to analog comparator or ADC (as an internal wire and without S/H stage)
- Two PDC channels
- Power reduction mode

12.12 Static Memory Controller

- 16-Mbyte Address Space per Chip Select
- 8- bit Data Bus
- Word, Halfword, Byte Transfers
- Programmable Setup, Pulse And Hold Time for Read Signals per Chip Select
- Programmable Setup, Pulse And Hold Time for Write Signals per Chip Select
- Programmable Data Float Time per Chip Select
- External Wait Request
- Automatic Switch to Slow Clock Mode
- Asynchronous Read in Page Mode Supported: Page Size Ranges from 4 to 32 Bytes
- NAND FLASH additional logic supporting NAND Flash with Multiplexed Data/Address buses
- Hardware Configurable number of chip select from 1 to 4
- Programmable timing on a per chip select basis

12.13 Analog Comparator

- One analog comparator
- High speed option vs. low power option
- Selectable input hysteresis:
 - 0, 20 mV, 50 mV
- Minus input selection:
 - DAC outputs
 - Temperature Sensor
 - ADVREF
 - AD0 to AD3 ADC channels
- Plus input selection:
 - All analog inputs
- output selection:
 - Internal signal
 - external pin
 - selectable inverter
- Interrupt on:
 - Rising edge, Falling edge, toggle

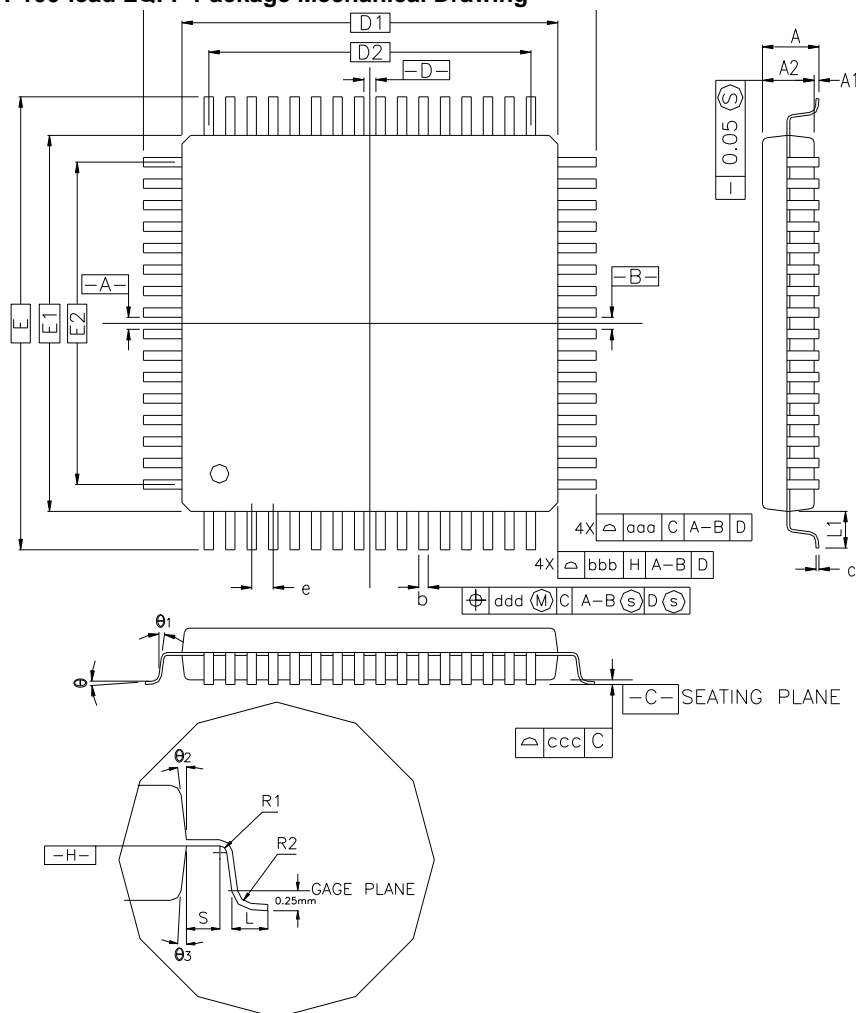
12.14 Cyclic Redundancy Check Calculation Unit (CRCCU)

- 32-bit cyclic redundancy check automatic calculation
- CRC calculation between two addresses of the memory

13. Package Drawings

The SAM3S series devices are available in LQFP, QFN and TFBGA packages.

Figure 13-1. 100-lead LQFP Package Mechanical Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---------------------------------|------------|------|------|------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A ₁ | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A ₂ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 16.00 BSC. | | | 0.630 BSC. | | |
| D ₁ | 14.00 BSC. | | | 0.551 BSC. | | |
| E | 16.00 BSC. | | | 0.630 BSC. | | |
| E ₁ | 14.00 BSC. | | | 0.551 BSC. | | |
| R ₂ | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| R ₁ | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 0.28° |
| θ ₁ | 0° | — | — | 0° | — | — |
| θ ₂ | 11° | 12° | 13° | 11° | 12° | 13° |
| θ ₃ | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L ₁ | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.010 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D ₂ | 12.00 | | | 0.472 | | |
| E ₂ | 12.00 | | | 0.472 | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.

Figure 13-2. 100-ball TFBGA Package Drawing

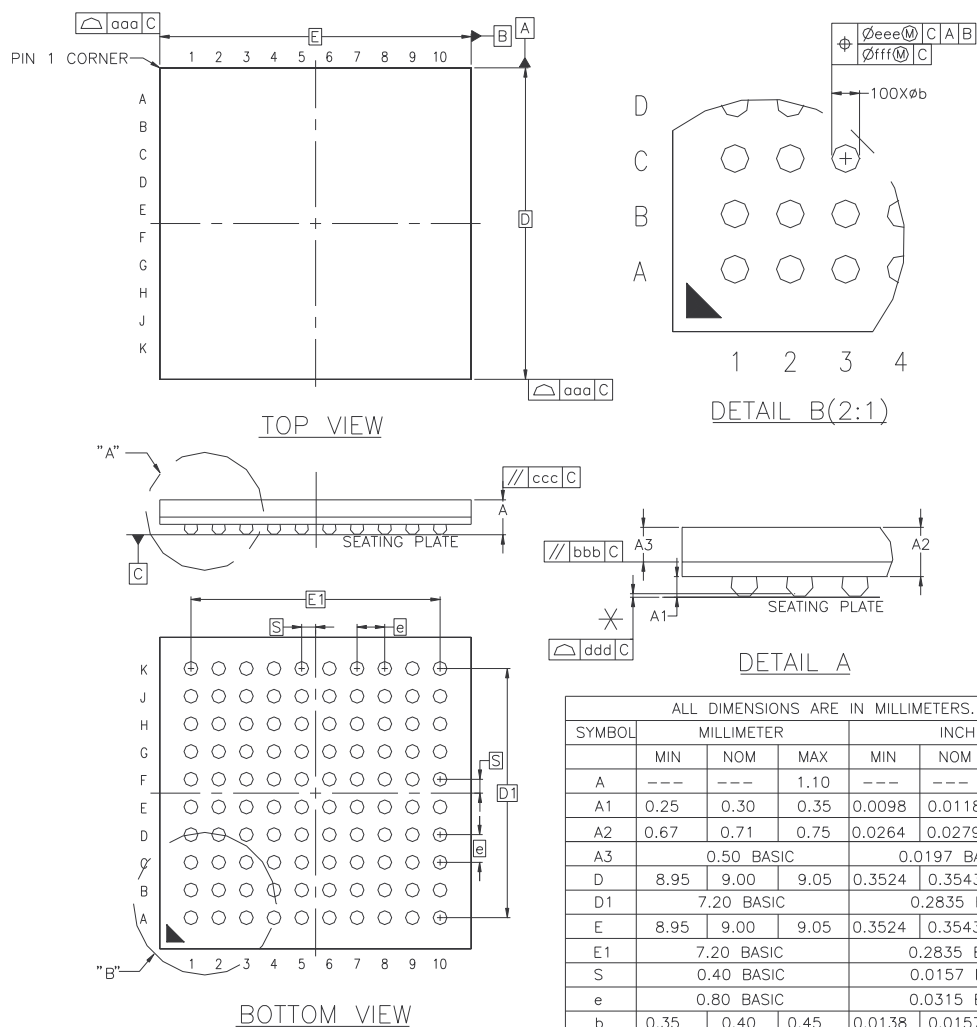


Figure 13-3. 64- and 48-lead LQFP Package Drawing

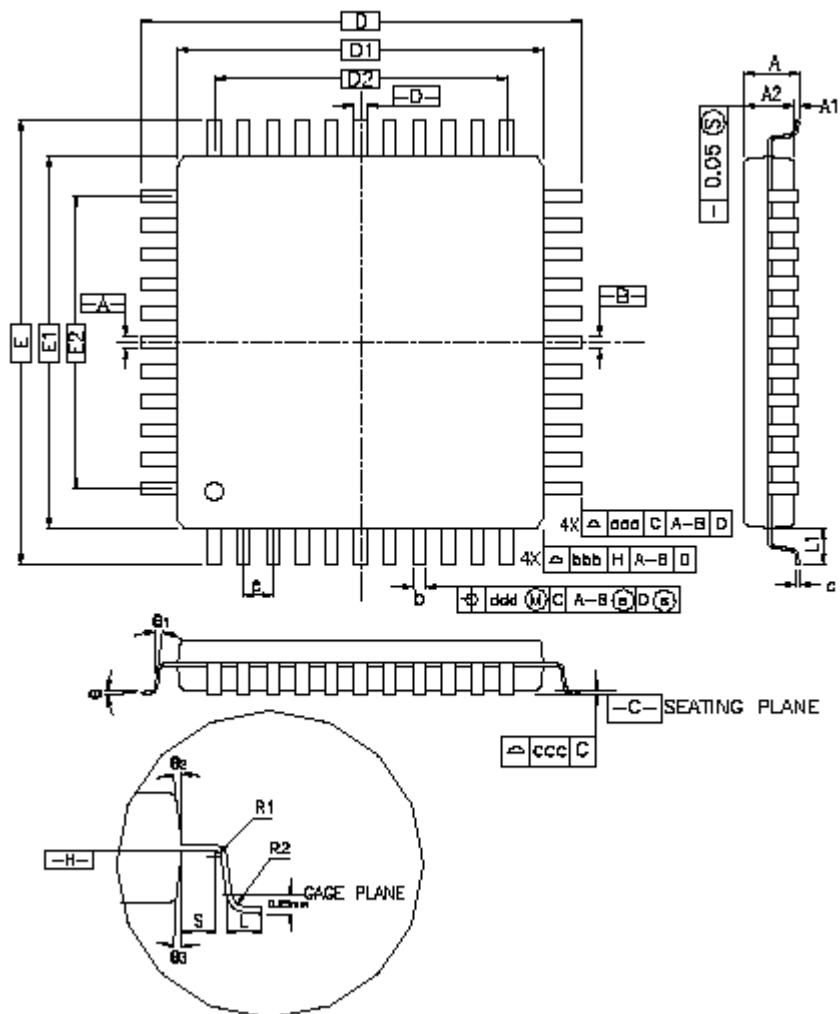


Table 13-1. 48-lead LQFP Package Dimensions (in mm)

| Symbol | Millimeter | | | Inch | | |
|---------------------------------|------------|------|------|------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 9.00 BSC | | | 0.354 BSC | | |
| D1 | 7.00 BSC | | | 0.276 BSC | | |
| E | 9.00 BSC | | | 0.354 BSC | | |
| E1 | 7.00 BSC | | | 0.276 BSC | | |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| R1 | 0.08 | — | — | 0.003 | — | — |
| q | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ ₁ | 0° | — | — | 0° | — | — |
| θ ₂ | 11° | 12° | 13° | 11° | 12° | 13° |
| θ ₃ | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 5.50 | | | 0.217 | | |
| E2 | 5.50 | | | 0.217 | | |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

Table 13-2. 64-lead LQFP Package Dimensions (in mm)

| Symbol | Millimeter | | | Inch | | |
|---------------------------------|------------|------|------|------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | – | – | 1.60 | – | – | 0.063 |
| A1 | 0.05 | – | 0.15 | 0.002 | – | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 12.00 BSC | | | 0.472 BSC | | |
| D1 | 10.00 BSC | | | 0.383 BSC | | |
| E | 12.00 BSC | | | 0.472 BSC | | |
| E1 | 10.00 BSC | | | 0.383 BSC | | |
| R2 | 0.08 | – | 0.20 | 0.003 | – | 0.008 |
| R1 | 0.08 | – | – | 0.003 | – | – |
| q | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ ₁ | 0° | – | – | 0° | – | – |
| θ ₂ | 11° | 12° | 13° | 11° | 12° | 13° |
| θ ₃ | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | – | 0.20 | 0.004 | – | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | – | – | 0.008 | – | – |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 7.50 | | | 0.285 | | |
| E2 | 7.50 | | | 0.285 | | |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

Figure 13-4. 48-pad QFN Package

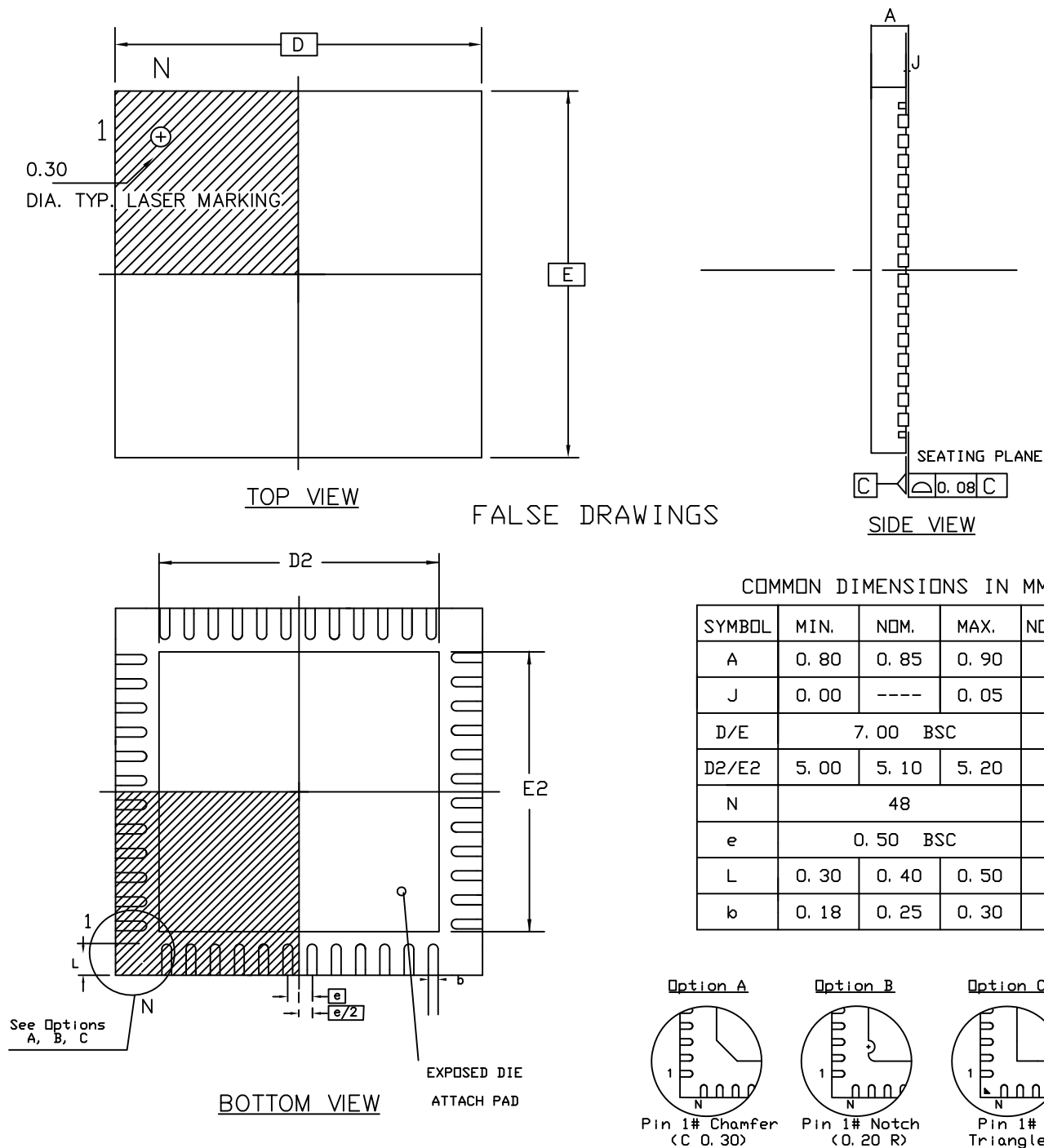
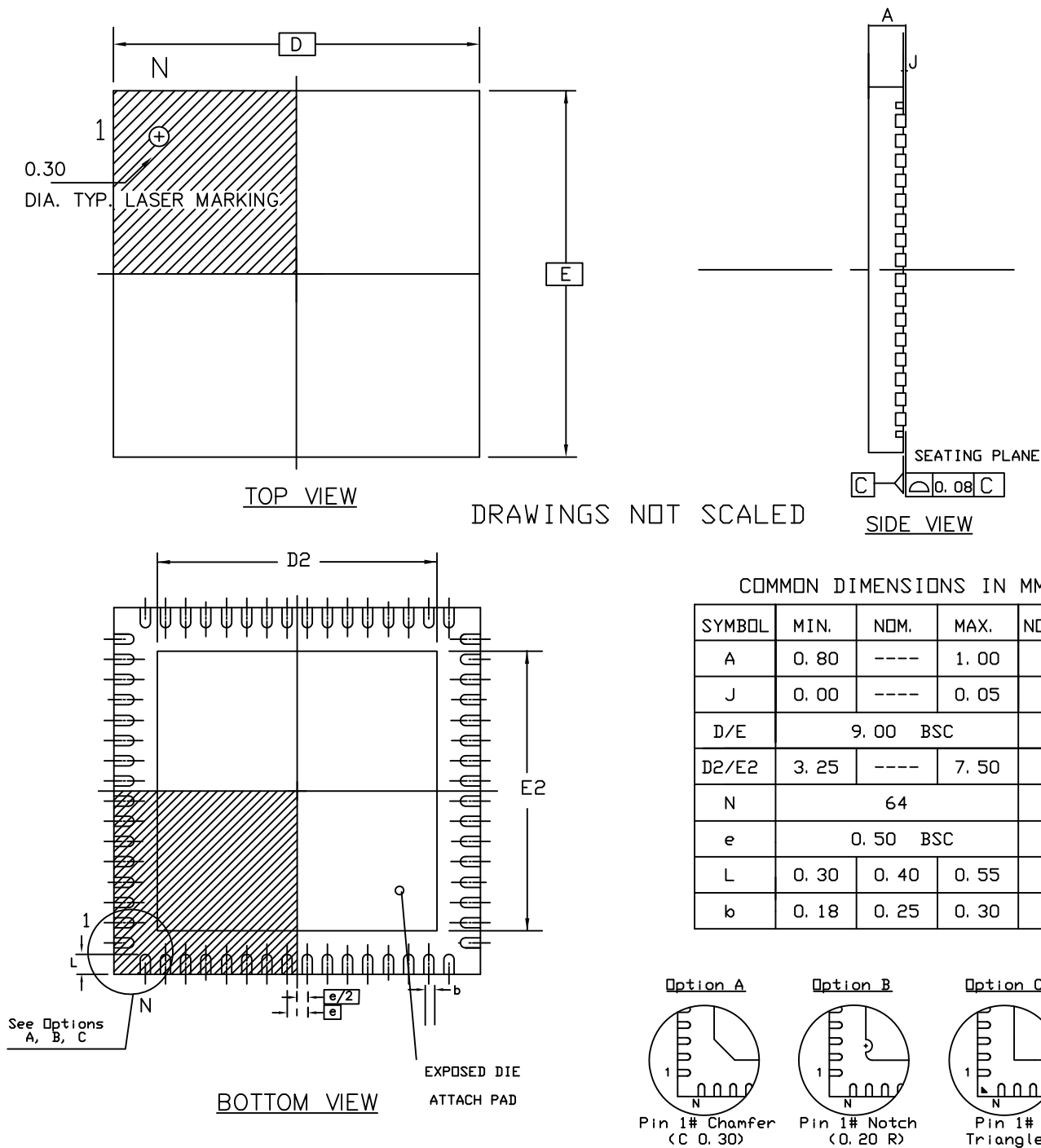


Table 13-3. 48-pad QFN Package Dimensions (in mm)

| Symbol | Millimeter | | | Inch | | |
|---------------------------------|------------|------|-------|-----------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | – | – | 090 | – | – | 0.035 |
| A1 | – | – | 0.050 | – | – | 0.002 |
| A2 | – | 0.65 | 0.70 | – | 0.026 | 0.028 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.18 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |
| D | 7.00 bsc | | | 0.276 bsc | | |
| D2 | 5.45 | 5.60 | 5.75 | 0.215 | 0.220 | 0.226 |
| E | 7.00 bsc | | | 0.276 bsc | | |
| E2 | 5.45 | 5.60 | 5.75 | 0.215 | 0.220 | 0.226 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| e | 0.50 bsc | | | 0.020 bsc | | |
| R | 0.09 | – | – | 0.004 | – | – |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.10 | | | 0.004 | | |
| ccc | 0.05 | | | 0.002 | | |

Figure 13-5. 64-pad QFN Package Drawing



14. Ordering Information

Table 14-1. Ordering Codes for SAM3S Series Devices

| Ordering Code | MRL A | MRL B | Flash (Kbytes) | Package (Kbytes) | Package Type | Temperature Operating Range |
|---------------|-------|-------|----------------|------------------|--------------|-----------------------------|
| ATSAM3S4CA-AU | A | – | 256 | QFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3S4CA-CU | A | – | 256 | BGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3S4BA-AU | A | – | 256 | QFP64 | Green | Industrial -40°C to 85°C |
| ATSAM3S4BA-MU | A | – | 256 | QFN64 | Green | Industrial -40°C to 85°C |
| ATSAM3S4AA-AU | A | – | 256 | QFP48 | Green | Industrial -40°C to 85°C |
| ATSAM3S4AA-MU | A | – | 256 | QFN48 | Green | Industrial -40°C to 85°C |
| ATSAM3S2CA-AU | A | – | 128 | QFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3S2CA-CU | A | – | 128 | BGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3S2BA-AU | A | – | 128 | QFP64 | Green | Industrial -40°C to 85°C |
| ATSAM3S2BA-MU | A | – | 128 | QFN64 | Green | Industrial -40°C to 85°C |
| ATSAM3S2AA-AU | A | – | 128 | QFP48 | Green | Industrial -40°C to 85°C |
| ATSAM3S2AA-MU | A | – | 128 | QFN48 | Green | Industrial -40°C to 85°C |
| ATSAM3S1CA-AU | A | – | 64 | QFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3S1CA-CU | A | – | 64 | BGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3S1BA-AU | A | – | 64 | QFP64 | Green | Industrial -40°C to 85°C |
| ATSAM3S1BA-MU | A | – | 64 | QFN64 | Green | Industrial -40°C to 85°C |
| ATSAM3S1AA-AU | A | – | 64 | QFP48 | Green | Industrial -40°C to 85°C |
| ATSAM3S1AA-MU | A | – | 64 | QFN48 | Green | Industrial -40°C to 85°C |
| ATSAM3S1CB-AU | – | B | 64 | QFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3S1CB-CU | – | B | 64 | BGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3S1BB-AU | – | B | 64 | QFP64 | Green | Industrial -40°C to 85°C |
| ATSAM3S1BB-MU | – | B | 64 | QFN64 | Green | Industrial -40°C to 85°C |
| ATSAM3S1AB-AU | – | B | 64 | QFP48 | Green | Industrial -40°C to 85°C |
| ATSAM3S1AB-MU | – | B | 64 | QFN48 | Green | Industrial -40°C to 85°C |

Revision History

| Doc. Rev | Comments | Change Request Ref. |
|----------|---|---------------------|
| 6500ES | Section 1. "Features" updated, "Low Power Modes", Sleep and Backup modes, down to 1.8 μ A in Backup mode | rfo |
| | Figure 8-1, "SAM3S Product Mapping", SRAM associated 1 MByte bit band region mapping changed: 0x22000000 to 0x23FFFFFF. Document format updated, subsequently pagination changed Section 14. "Ordering Information" Introduced MRL B for SAM3S1 parts.. | 8545 |
| 6500DS | Replace all mention to 100-ball LFBGA into 100-ball TFBGA. | 8044 |
| | Add table note 5 in Table 3-1, "Signal Description List". | 7632 |
| | Add MOSCRCEN bit details in Section 5.5.2 "Wait Mode". | 7639 |
| | Section 9.1.3.9 "Fast Flash Programming Interface" updated. | 7668-7901 |
| | Notes under Figure 5-1, "Single Supply" and Figure 5-2, "Core Externally Supplied" modified. | 7887 |
| | Cross-References (1) added for 64-pin packages in table Table 1-1, "Configuration Summary". | 8033 |
| | Pin 22 value changed for PA23/PGMD11 in Table 4-1, "100-lead LQFP SAM3S4/2/1C Pinout". | 8093 |
| | "High Frequency Asynchronous clocking mode" removed from Section 12.7 "Pulse Width Modulation Controller (PWM)" | 8095 |
| 6500CS | "Write Protected Registers" added in "Description", in Peripherals list. | 8213 |
| | ADC column values updated in Table 1-1, "Configuration Summary". | rfo |
| | Missing PGMD8 to 15 added to Table 4-1, "100-lead LQFP SAM3S4/2/1C Pinout" and Table 4-2, "100-ball TFBGA SAM3S4/2/1C Pinout". | rfo |
| | Section 5.7 "Fast Startup" updated. | 7536 |
| | Typo fixed on back page: 'techincal' --> 'technical'. | 7524 |
| | Typos fixed in Section 1. "Features". | |
| | Missing title added to Table 14-1. | 7494 |
| | PLLA input frequency range updated in Section 10.5 "Clock Generator". | 7492 |
| 6500BS | A sentence completed in Section 5.5.2 "Wait Mode". | 7428 |
| | Last sentence removed from Section 9.1.3.10 "SAM-BA® Boot". | |
| | 'three GPNVM bits' replaced by 'two GPNVM bits' in Section 9.1.3.11 "GPNVM Bits". | |
| | Leftover sentence removed from Section 4.1 "SAM3S4/2/1C Package and Pinout". | 7394 |
| | "Packages" on page 2, package size or pitch updated. | |
| | Table 1-1, "Configuration Summary", ADC column updated, footnote gives precision on reserved channel. | 7214 |
| | Table 4-2, "100-ball TFBGA SAM3S4/2/1C Pinout", pinout information is available. | 6981 |
| | Figure 5-1, "Single Supply", Figure 5-2, "Core Externally Supplied", updated notes below figures. | 7201 |
| 6500AS | Figure 5-2, "Core Externally Supplied", Figure 5-3, "Backup Battery", ADC, DAC, Analog Comparator supply is 2.0V-3.6V. | 7243/rfo |
| | Section 12.13 "Analog Comparator", "Peripherals" on page 2, reference to "window function" removed. | 7103 |
| | Section 9.1.3.8 "Unique Identifier", Each device integrates its own 128-bit unique identifier. | 7307 |
| 6500AS | First issue | |



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