TECHSEM

BCA50

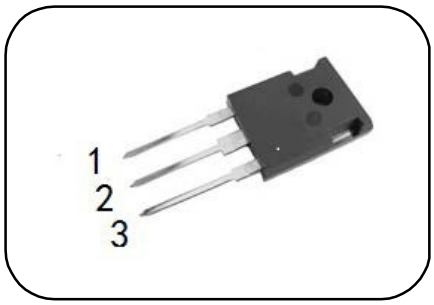
Features

- **n** Thyristor for line frequency
- **n** Planar passivated chip
- **n** Long-term stability

Typical Applications

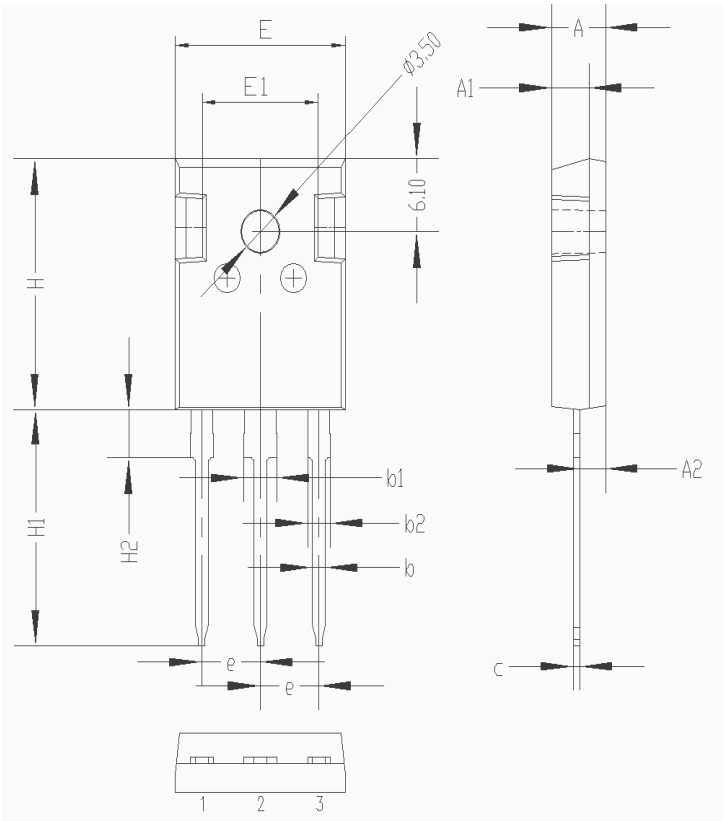
- **n** High power industrical and power transmissior
- **n** DC and AC motor control
- **n** AC controllers

$I_{T(AV)}$	**50A**	
V_{DRM}/V_{RRM}	**1200V**	
I_{TSM}	**600**	**A**
I^2t	**1800**	**A^2s**



SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T_j(°C)	VALUE			UNIT
					Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,	T_C= 80°C	125			50	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM}, tp=10ms		125			1200	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM}		125			10	mA
		at V_{RRM}		25			100	uA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}		125			600	A
I^2t	I^2t for fusing coordination						1800	A^2s
V_{TO}	Threshold voltage			125			0.9	V
r_T	On-state slope resistance						6.2	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=50A		25			1.4	V
		I_{TM}=110A		25			1.8	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}		125	1000			V/μs
di/dt	Critical rate of rise of on-state current	V_{DM}= 67%V_{DRM} to 800A, Gate pulse t_r ≤0.5μs I_{GM}=1.5A Repetitive		125		100		A/μs
C_J	Junction capacitance	V_R=400V, f=1MHz		25		23		pF
I_L	Latching current	I_G=1.2 I_{GT}					200	mA
I_{GT}	Gate trigger current	V_A=12V, I_A=1A		25			100	mA
V_{GT}	Gate trigger voltage						1.8	V
I_H	Holding current						150	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=0.67V_{DRM}		125	0.25			V
$R_{th(j-c)}$	Thermal resistance Junction to case	At 180^0 sine, double side cooled Clamping force 7.0kN					0.3	°C /W
T_{stg}	Stored temperature				-40		150	°C
Outline	TO-247							

Outline:



	单位 mm		
	MIN	NOM	MAX
A	4.8	5	5.2
A1	3.3	3.5	3.7
A2	2.1	2.3	2.5
b	1	1.2	1.4
b1	2.9	3.1	3.3
b2	1.9	2.1	2.3
c	0.4	0.6	0.8
e	5.25	5.45	5.65
E	15.6	15.8	16
E1	10.6	10.8	11
H	20.8	21	21.2
H1	19.4	19.9	20.4
H2	3.9	4.1	4.3
G	5.9	6.1	6.3
ØP	3.3	3.5	3.7